INTEGRATOR CIRCUITRY USED TO DETERMINE THE RADIAL PROFILE OF A NON-NEUTRAL PLASMA

by

Colby J. Dawson

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DEPARTMENT APPROVAL

of a senior thesis submitted by

Colby J. Dawson

This thesis has been reviewed by the research advisor, research coordinator, and department chair and has been found to be satisfactory.

Date	Bryan Peterson, Advisor
Date	Eric Hintz, Research Coordinator
Date	Ross Spencer, Chair

ABSTRACT

INTEGRATOR CIRCUITRY USED TO DETERMINE THE RADIAL PROFILE OF A NON-NEUTRAL PLASMA

Colby J. Dawson

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In order to determine the relative ion density in a confined, non-neutral plasma, I have designed and built circuitry used to add up the amount of charge in nine annular regions expanding radially outward from the axis of the confinement region. The plasma is dumped by grounding the side of the confinement system closest to charge-collecting rings, causing ions to collect on each region. Accumulating charges cause a current to flow to a corresponding integrator circuit where the amount of charge on each region is quantified. A sample-and-hold circuit is appended to each integrator circuit to minimize error due to output drift. The integrator circuits are externally read and controlled by computer through a logic circuit.

Ion density information will be used to fine-tune system confinement parameters to retain as many ions as possible.

ACKNOWLEDGMENTS

I'd like to thank Dr. Peterson for getting me started on this project and helping to bring it to this point. Obviously, it would have been impossible to carry out without his bounteous help. I'm grateful to the BYU Physics Department as a whole for making the undergraduate research experience possible as well as providing an exceptional and rewarding undergraduate education.

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Chapter 1

Introduction

1.1 Background

This project is part of a larger project to measure the half-life of ionized Beryllium 7. ^{7}Be is interesting because it is the lightest radioactive element which decays exclusively by electron capture. In the process, an electron is captured by a proton in the nucleus forming the decay product ^{7}Li as well as a neutrino.

Neutral ^{7}Be has a relatively well-defined half-life of 53 days. However, variations in the half-life of ^{7}Be have been observed by several researchers, particularly when embedded in other substances[1]. It is hypothesized that ionization affects the half-life of the element by reducing electron density around the nucleus, thus decreasing the decay rate by about 5%. Ionization effects on half-life have been observed in the higher-order radioactive element ^{140}Pr when fully ionized[2]. The study of these effects on half-life is likely to be effective using ^{7}Be since ionization takes place in the s-shell from which electrons are captured during decay. In higher-order elements which decay by electron capture, ionization takes place in outer shells such that s-shell electrons are unaffected.

On 12 January 1990, the Long Duration Exposure Facility which had been orbiting the earth in the upper atmosphere was retrieved from orbit. Experimental results revealed that the surface of the spacecraft contained approximately 1000 times the expected amount of ^{7}Be, puzzling researchers[3]. The original motivation for our project was to determine if ionization of ^{7}Be by cosmic rays in the upper atmosphere could account for the increased amount of ^{7}Be found on the spacecraft.

1.2 Description of Group Project

The experimental non-neutral plasma group at Brigham Young University is building a Malmberg-Penning trap in which to confine a ^{7}Be ion plasma for several months. ^{7}Be is produced by bombarding boron carbide (enriched to 93% ^{10}B) with a 400 KeV proton beam in a Van de Graaff accelerator. Protons collide with ^{10}B producing ^{11}C which undergoes alpha decay to become ^{7}Be. The target with embedded ^{7}Be is then transferred to the confinement system and ionized by vacuum arc.

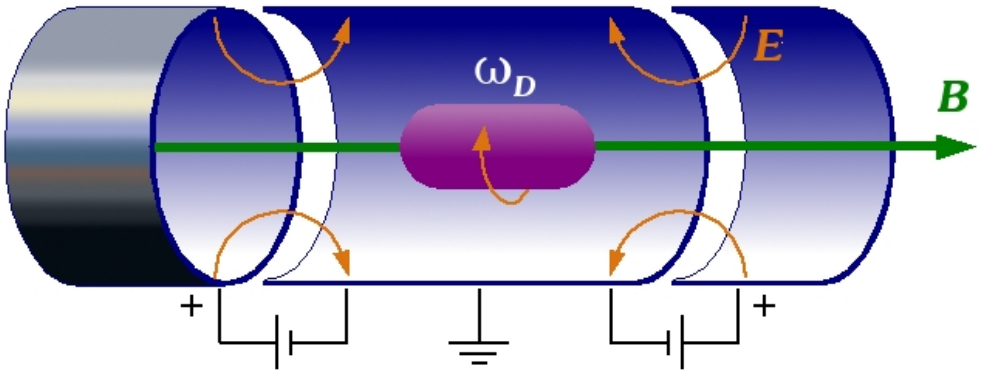

Figure 1.1: A Malmberg-Penning trap

The plasma enters the pumped-down confinement chamber through a quadrupole which filters ionized contaminants from the plasma and channels ^{7}Be ions into the

magnetic field of the confinement system.

The ion plasma tends to expand outward in the confinement system due to Coulomb repulsion. To neutralize this effect, the plasma is to be confined axially in the system by an electrostatic potential well and radially by a magnetic field along the machine axis as shown in Figure 1.1. The potential well also serves to remove any free electrons which would neutralize the ^{7}Be ions.

Ions slowly drift outward in the system due to collisions with neutral particles. A rotating wall system, consisting of a time-dependent dipole or quadrupole electric field, will be designed to compress the plasma and prevent ions from colliding with the outer wall of the chamber.

The relative concentrations of ^{7}Be and its decay product ^{7}Li are to be determined by Fourier Transform Ion Cyclotron Resonance Mass Spectrometry.

In order to determine the density of ions in the confinement system, I designed and built circuitry used to add up the amount of charge in nine annular regions expanding radially outward from the axis of the confinement region (see Figures 1.2, 1.3). The ions are dumped by grounding the potential on the side of the confinement chamber closest to the charge-collecting rings. As ions collect on each annular region, a current is generated which flows to various integrator circuits where the amount of charge on each region is quantified. The amount of charge collected on each annulus is directly proportional to the number of ions in each region. Knowing the volume of each region, the ion density in each individual region can be determined. Thus it will be possible to characterize the system and fine-tune confinement parameters to retain as much of the original plasma as possible. Optimally, the plasma will be most concentrated in the inner regions where there is no risk of ions colliding with the outer wall and becoming neutralized.

At this point, the ion source has been designed and fabricated and the quadrupole

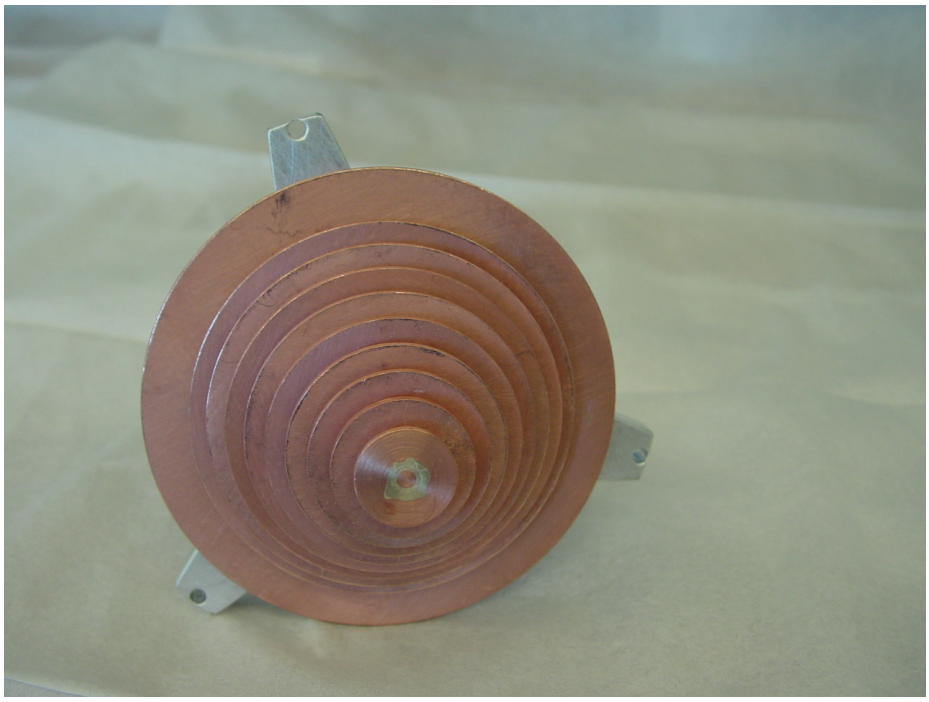

Figure 1.2: The charge collecting rings viewed from along the machine axis. Each ring corresponds to a cylindrical shell volume in the confinement system.

is nearly completed. Most of the confinement system hardware is in place. Necessary future work includes the design and fabrication of circuitry to control confinement parameters.

1.3 Thesis Outline

In the following chapters, the design and fabrication of the circuit will be described in detail. The control mechanism for the circuit will be described and data taken during characterization of the circuit will be presented.

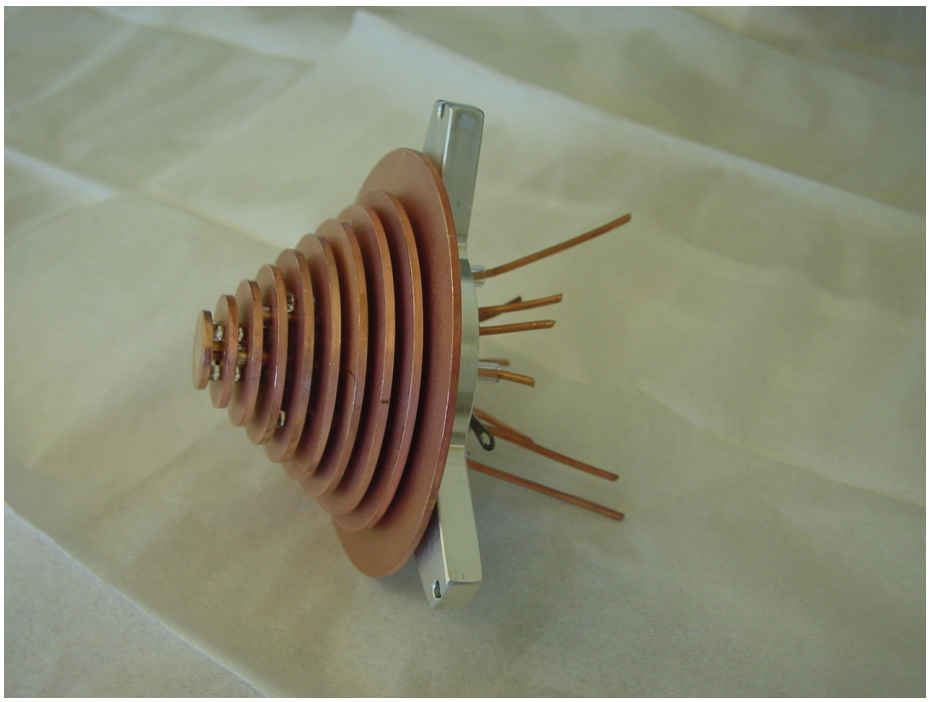

Figure 1.3: The charge collecting rings viewed from the side.

Chapter 2

Details

2.1 Integrator Circuit Design

Integrator circuits work by allowing charge entering the circuit to build up on a capacitor. The measured voltage output of the circuit corresponds to the amount of capacitor charge by the simple relation $Q = C\Delta V$.

A simple integrator involves a resistor in series with a capacitor attached to ground. The main problems with such an integrator are attenuation of the input signal and high output impedance. Adding an operational amplifier to the circuit remedies the problems by lowering the output impedance and amplifying the input signal.[4]

The integrator circuit was designed with several important considerations. First, it was necessary that the amplifier used in the circuit have a high input impedance. This ensured that all charge entering the circuit accumulated on the integrator capacitor rather than being lost to ground through the amplifier. Second, it was necessary that the amplifier have a high slew rate (response rate) since the signal was to be read from the integrators in rapid succession. Third, it was necessary that the amplifier

have a low bias current from the negative input. The bias current tends to counteract the current entering the circuit, charging the integrator capacitor and thus causing the output to drift. We eventually selected the Linear Technologies LT1169 Op Amp under these considerations. The LT1169 has JFET inputs (high impedance), featuring low input bias current[5] as necessary for our measurements.

We also found it necessary to include a large resistor in parallel with the integrator capacitor to increase stability in the circuit. However, the resistor has the effect of slowly discharging the integrator capacitor (time constant 0.5 ms), causing output drift. An analog switch across the integrator capacitor allows the integrator to be cleared as necessary. We found the ADG412 analog switch sufficient for our purposes[6].

2.2 Sample-and-Hold Circuit

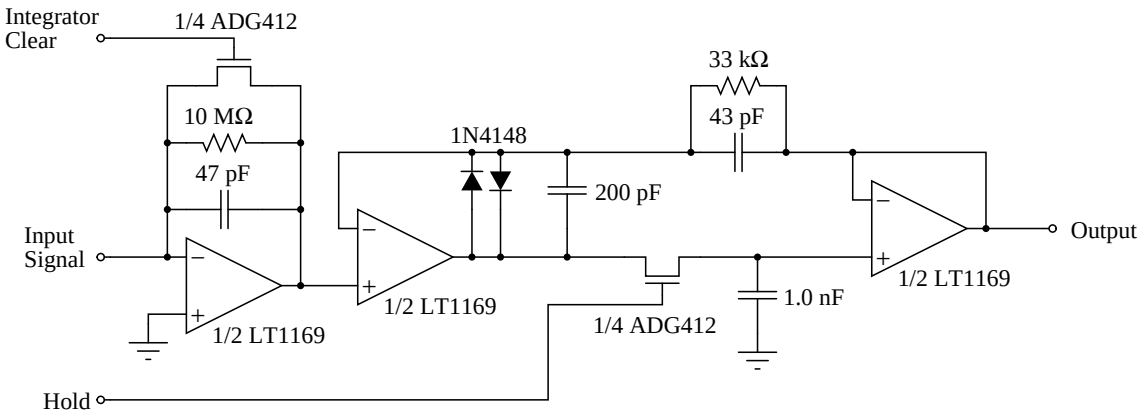

Figure 2.1: Schematic of Integrator and Sample-and-Hold Circuit

Because of significant drift in the output of the integrator circuit, it was advantageous to append a sample-and-hold circuit to each integrator. When activated, the sample-and-hold circuit holds the output from the integrator circuit with minimal

drift. This action requires opening an analog switch in the sample-and-hold circuit. The sample-and-hold circuit is to be triggered at some point soon after the output of the integrator has sufficiently stabilized.

Design of the circuit was based on a prototype presented by J.B. Calbert[7]. Opening an analog switch in the circuit causes the input signal immediately preceding the action to be maintained as the voltage across a capacitor attached to ground. The ungrounded end of the capacitor is attached to the non-inverting input of the second amplifier such that the output of the amplifier reflects the voltage across the capacitor. If the switch remains closed, the sample-and-hold circuit transfers the input signal unaltered. Triggering the switch causes a small amount of charge to be injected into the circuit, charging the capacitor and thus affecting the output. In final calibration, we measured this effect at different input amplitudes to factor into later measurements.

As mentioned earlier, the output of the sample-and-hold circuit remains approximately constant, displaying extremely low drift due primarily to leakage current from the negative input of the second amplifier. This effect is quite small and approximately linear. This is in contrast to the output drift of the integrator which is significant and relatively difficult to predict. It is possible to command hold in each circuit simultaneously and because the outputs of circuits must be measured in succession, we can ensure that these measurements correspond in time. This is the advantage of appending the sample-and-hold circuit to the integrator.

Amplifiers in the circuit prevent attenuation of the voltage signal while maintaining its value. Diodes in parallel connect the feedback loop to the output of the first amplifier, effectively maintaining the output when the switch is open. Resistors and capacitors in the feedback loop are necessary to maintain stability in the circuit[7]. We used the circuit simulation program LTSPICE[8] to test various capacitor values

for maximum circuit stability.

To test the actual circuit the various components were ordered and assembled on a breadboard. A pulse generator was attached to the hold switch in the sample-and-hold circuit, opening the switch soon after the integrator output had stabilized. We externally triggered the oscilloscope from the signal generator such that the signal was displayed at the point of interest. We then read and recorded the oscilloscope trace using a virtual instrument in LabVIEW and graphed the trace values using the software, MATLAB. A sample trace is shown in Figure 2.2. Data from initial circuit characterization is found in Table A.1 in the appendix.

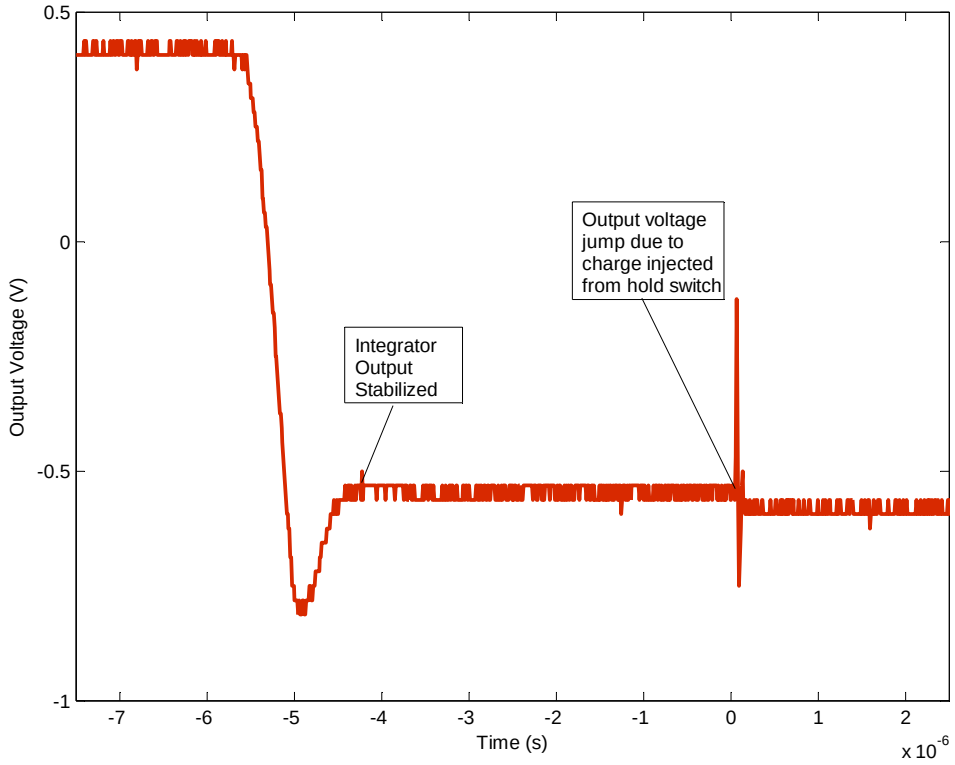

Figure 2.2: Oscilloscope trace of output of sample-and-hold circuit for 500 mV input amplitude

We found that the circuit effectively integrated charge pulses produced by sending a square-wave signal through a capacitor. This was the most realistic simulation of

integrating charge on collection rings, and thus demonstrated that the circuit was sufficient for our purposes.

2.3 Logic to Control Circuits

Nine integrator and sample-and-hold combinations were built, each corresponding to a single charge-collecting ring. Three other combinations were built for other purposes in the confinement system. It was necessary to design additional circuitry allowing us to externally control the circuits from a computer and read the output of each integrator in succession.

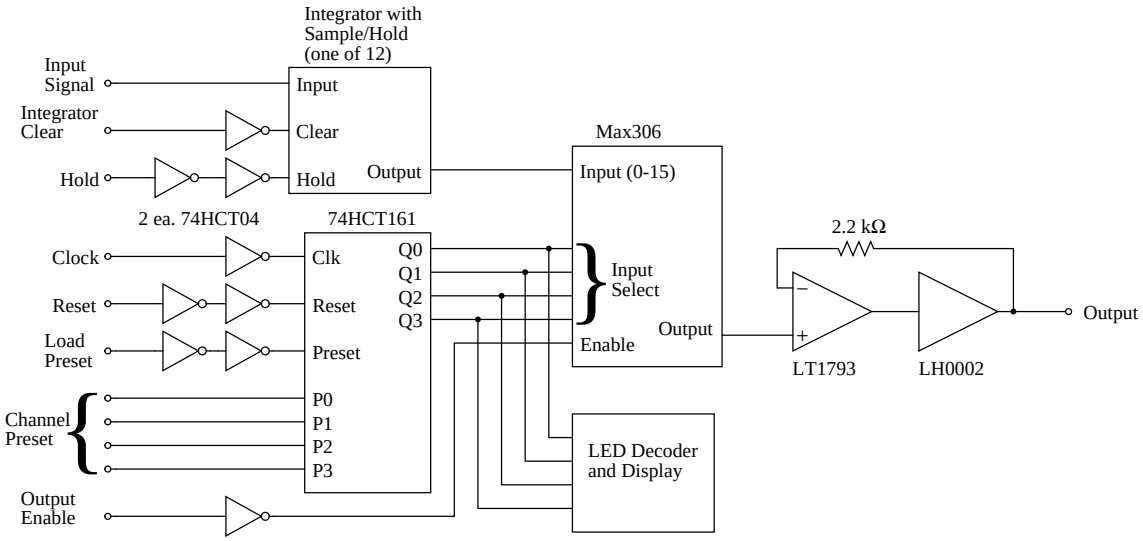

Figure 2.3: Schematic of Integrator and Sample-and-Hold Circuit

A multiplexer (MAX306) was implemented to sequentially multiplex the 12 integrator outputs onto a single output line. The common output of the multiplexer displays the voltage on the numbered input (NO1-16) corresponding to a binary input (A0-4).[9] A binary counter (74HCT161) was used to control the binary input of the multiplexer. When the clock input (Clk or CP on the data sheet) on the counter is

triggered from low to high, the counter cycles to the next consecutive binary output corresponding to numbers zero through fifteen. The counter may be reset at any time by triggering the reset input (Reset or MR on the data sheet). The 74HCT161 counter also has a preset value function[10]. A digital display was attached to the output of the counter, showing which integrator output corresponded to the output of the multiplexer.

It was necessary to create six input lines to the circuit from a computer. The computer interacts with the circuit by digital signals from a National Instruments multi-I/O board. The input lines are to be maintained at low voltage in order for the specific function controlled by the input lines to be performed. The input line functions are as follows.

The "clear integrator" line triggers the analog switch which clears the capacitors in the integrator circuit. Since the switch is closed for a high voltage signal, it was necessary to connect the "clear integrator" line through an inverter gate. The inverter gate also acts as a driver, allowing the signal to meet the current requirement necessary to trigger the switches in all twelve integrator circuits. We selected a standard 74HCT04 hex-inverter[11].

As soon as the amplifier in the integrator receives power, it begins to leak bias current charging the integrator capacitor. As a result, the capacitors in the integrator circuits must be cleared of charge immediately before measurements are taken. This is to ensure that the amount of charge which accumulates on the capacitors accurately reflects that on the charge-collecting rings when the plasma is dumped.

The "hold" line triggers the switch in the sample-and-hold circuit. Since the switch is to be open when the hold function is performed (opposite the "clear integrator" switch), it was necessary to connect the "hold" line through two inverter gates. These gates also drive the signal to meet the current requirement of the twelve switches.

Because the hold line is connected to all 12 integrator circuits, it is possible to command hold in each circuit simultaneously, as mentioned earlier. This ensures that all integrator measurements correspond in time, reducing complexity in data analysis.

The "clock" line is attached to the "Clk" input of the counter. When the input voltage is brought from low to high, the binary output of the counter (and thus the binary input to the multiplexer) changes to the next highest value. This makes it possible to call the output from each integrator in succession after commanding hold. The "clock" line is connected through a single inverter gate.

The "reset" line is attached to the "Reset" input of the counter. When the input voltage is high, the binary output of the counter is reset to zero, making it possible to cycle through the integrator outputs again. The "reset" line is connected through two inverter gates.

The "preset value" line is attached to the "Preset" input (or SPE on the data sheet) of the counter. When the input voltage is low and the "Clk" input of the counter is brought from low to high, the preset binary value (P0-3) becomes the output of the counter. This makes it possible to call the output of the single integrator circuit not attached to the charge collectors. The "preset value" line is connected through two inverter gates.

The "output enable" line is attached to the "Enable" input (or EN on the data sheet) of the multiplexer. When the input voltage is high, the multiplexer is functional. The "output enable" line is connected through a single inverter gate.

A virtual instrument was designed in LabVIEW to control each specific circuit function from the computer.

2.4 Designing and Assembling the Circuit Board

With preliminary designs completed, it became possible to assemble a board for the physical circuit. We elected to use the software program PCB123[12] to convert a schematic diagram to a block diagram representing the physical layout of the circuit board as shown in Figure 2.4.

Since the LT1169 chip is a dual amplifier, we found it convenient to share one of the chips between integrator circuits. Each ADG 412 chip includes four switches to be shared between two integrator/sample-and-hold combinations.

Once completed, we submitted the board layout to Sunstone Circuits. The circuit board was then fabricated as designed (without actual components) and sent to us by mail.

Once the board was received, the individual components were soldered in place. A box was designed and fabricated on which to mount the circuit. A power supply was also built into the box such that the entire instrument was self-contained. Coaxial cables with grounded sheaths were used to connect the input signal of each individual integrator circuit.

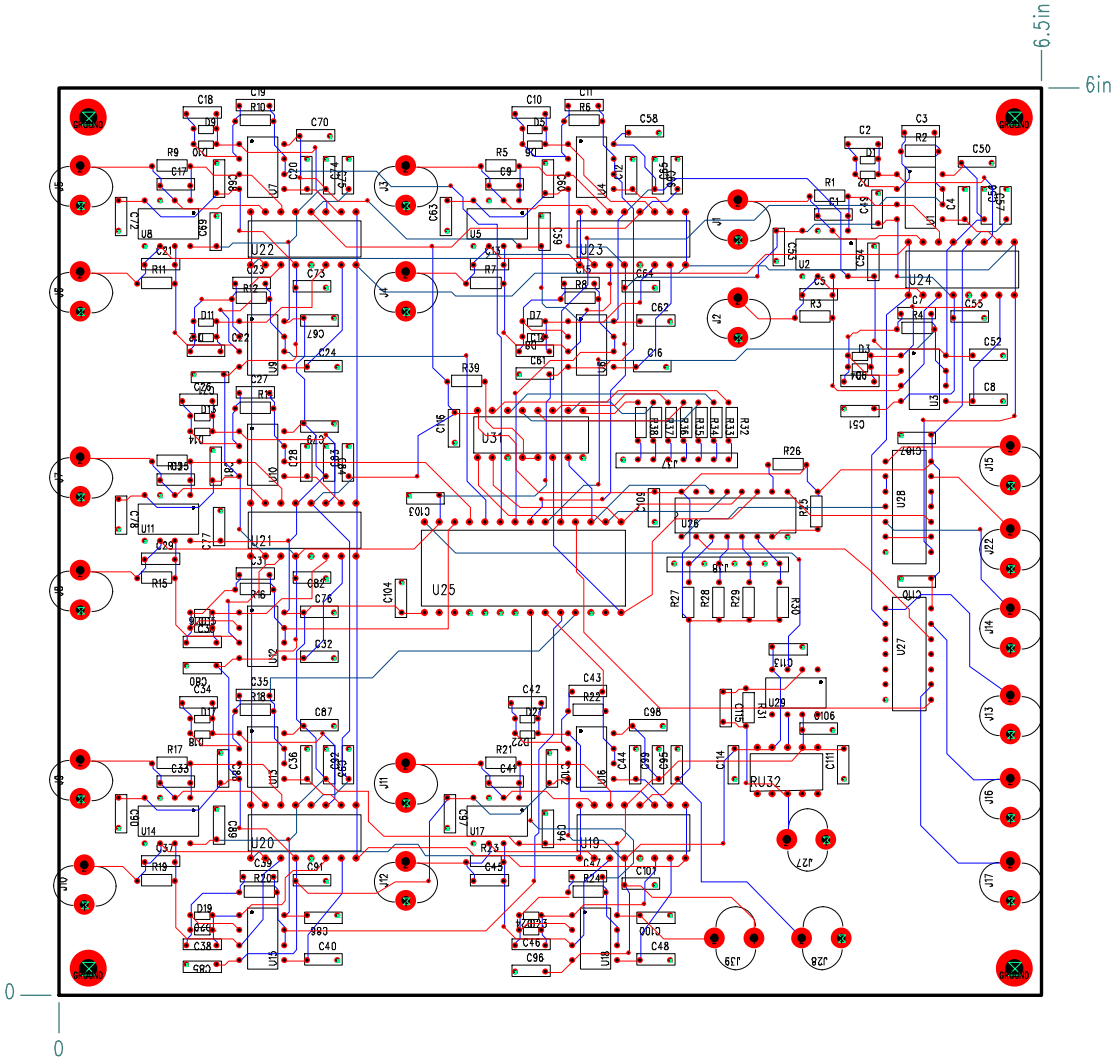

Figure 2.4: Layout diagram of circuit generated on PCB123 LAYOUT. Red corresponds to the top layer of the board. Blue corresponds to the bottom layer. Dark blue corresponds to the second interior layer. The first interior layer, which is a ground plane, is not shown.

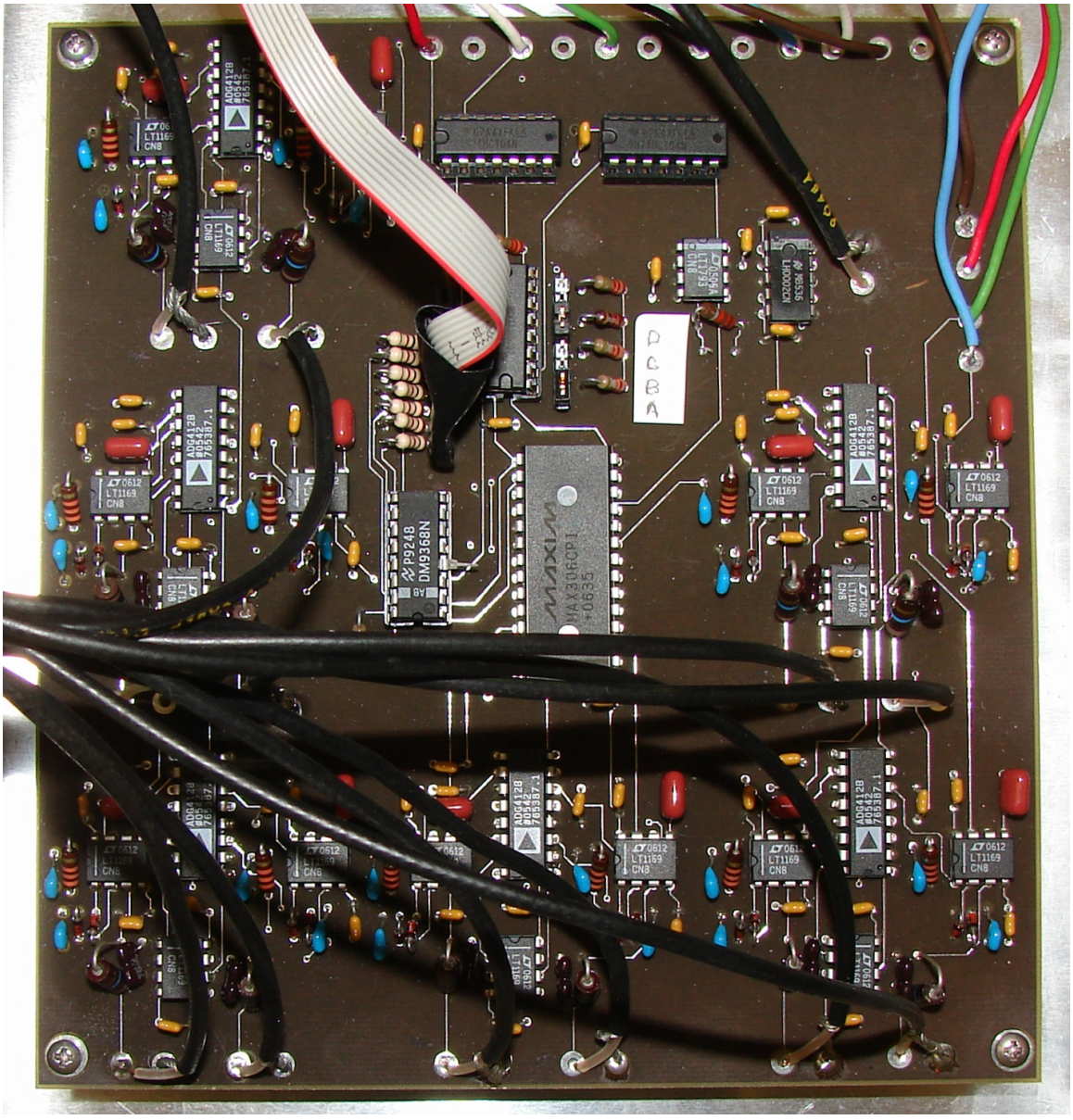

Figure 2.5: Photograph of the actual circuit board. Each of the six identically patterned circuits on the outside corresponds to two integrator/sample-and-hold combinations. The large chip in the center is the multiplexer. The chip directly to the left of the multiplexer is the counter. The colored wires entering the top of the photograph are the lines in from the computer. The black coaxial cables entering the figure from the left are the inputs to each integrator.

Chapter 3

Results and Conclusions

3.1 Final Calibration

To calibrate the completed circuits, we constructed a setup similar to that used for initial calibration. The circuits integrated a charge pulse generated by sending a square wave through a capacitor. A virtual instrument was programmed in LabVIEW to send pulses to the hold switch on each circuit a small amount of time after the output of the integrator had stabilized, identical to the function of the pulse generator during initial circuit characterization.

An extensive calibration of the circuits was carried out from a computer. The computer controls the input to the circuit and monitors the output of the circuit simultaneously. We are able to scan the output for a wide range of input amplitudes and determine the relationship between the output and the input.

The value "V_{in}" (amplitude of the square wave input signal) is proportional to the charge entering the circuit by the relation $Q = CV_{in}$, where C=138 pF is the capacitance of the capacitor from which the charge pulse entering the circuit emerges. Because we have used a capacitor for which the capacitance was carefully measured

and is thus well-defined, the amount of charge entering the circuit is also well-defined. It is thus possible to compare the amount of charge entering the circuit with the amount of charge which accumulates on the integrator capacitor. The calibration is to determine how these two values correlate given the various factors affecting the output of the integrator. The amount of charge injected into the circuit is varied and each corresponding output measured to determine the relationship between charge injected into the circuit and output voltage of the circuit.

Figure 3.1 shows a sample output trace from one of the circuits. The value "$V1_{out}$-$V2_{out}$" is proportional to the amount of charge on the integrator capacitor according to $Q = CV$. The capacitance of the capacitor in each integrator circuit is approximately 47 pF but can vary by up to 10 % of this value. Leakage current from the negative input of the amplifier tends to charge the integrator capacitor, thus causing the output to drift. The resistor in parallel with the capacitor tends to discharge the capacitor also affecting the output.

The value "$V2_{out}$-$V3_{out}$" represents charge injected by opening the switch in the sample-and-hold circuit. We expect this value to remain constant for different input amplitudes.

We observed an approximately linear relationship between the charge pulse injected into the circuit through the 138 pF capacitor (proportional to V_{in}) and the charge across the integrator capacitor (proportional to $V1_{out}$-$V2_{out}$), as displayed in Figure 3.2. The area of most interest includes input voltages from 1.0-1.25 Volts (corresponding to 10^9 charges), since this is the amount of charge expected to accumulate on charge-collecting rings.

The magnitude of the charge injected by opening the hold switch causes a small offset in output measurements as seen by comparing Figures 3.2 and 3.3. The effect is very small, changing the total charge on the hold capacitor by approximately 1 %.

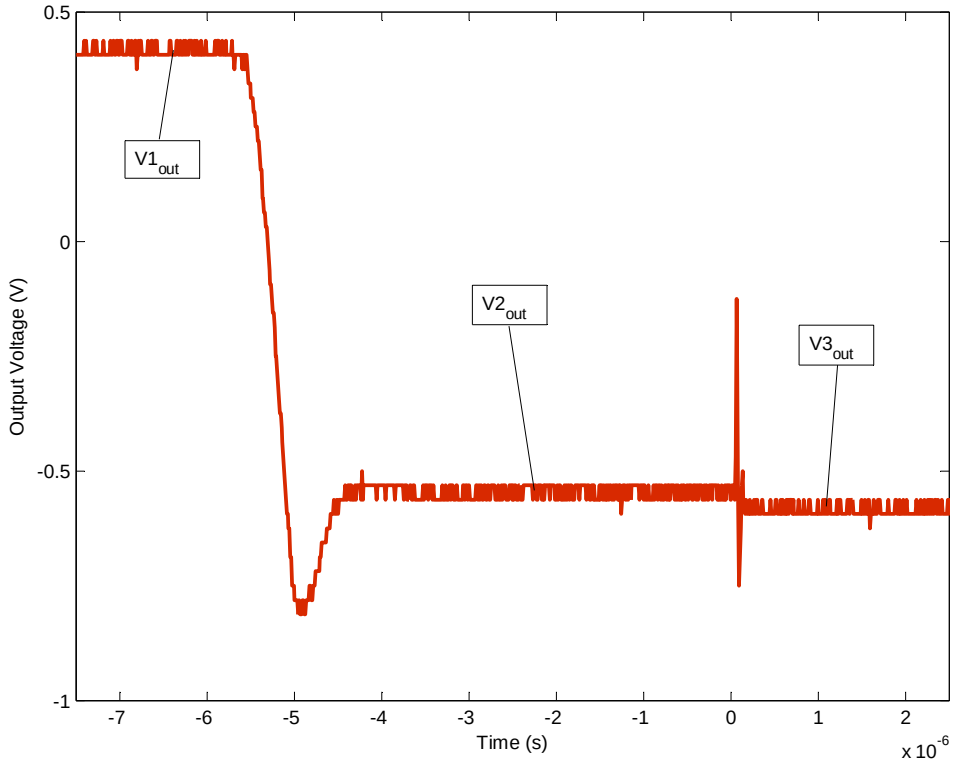

Figure 3.1: Oscilloscope trace of output of sample-and-hold circuit for 500 mV input amplitude

Data from the final calibration is tabulated in the Appendix.

3.2 Conclusion

We succeeded in producing a functional instrument for use in the plasma confinement system. Calibration of the circuits demonstrated a predictable relationship between the actual charge injected into the circuit and the output measurement. We found that we could determine the individual response of each of the twelve circuits, specifically the factor relating output voltage to charge injected into the circuit. This response was determined to be independent of charge input within the range of interest. We also found that the charge injected by activating the hold switch was approximately

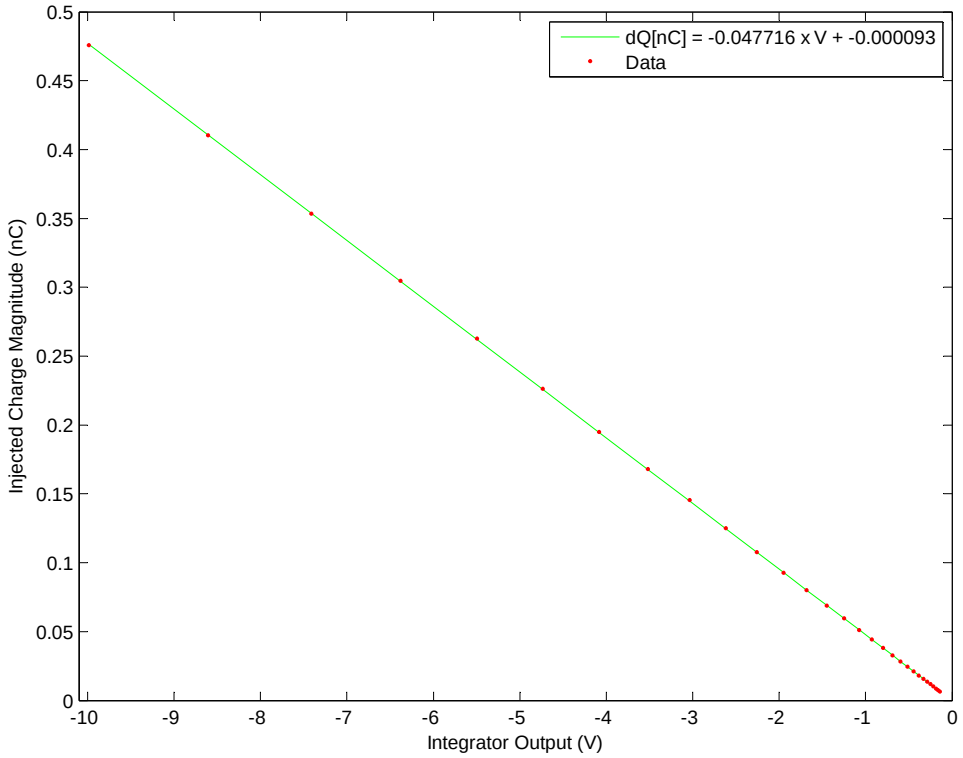

Figure 3.2: Relationship between charge injected into the circuit and output voltage of integrator

constant for all input voltages.

Further steps in calibration include measuring the drift rate of the integrators as well as that of the sample-and-hold circuits. This will be done by monitoring the output signal of the circuit without activating the hold switch and measuring the drift of the output.

Results of calibration are reproducible and demonstrate that we can be confident the output of the circuits when used to take actual measurements, accurately reflects the charge accumulated on each charge-collector ring in the confinement system.

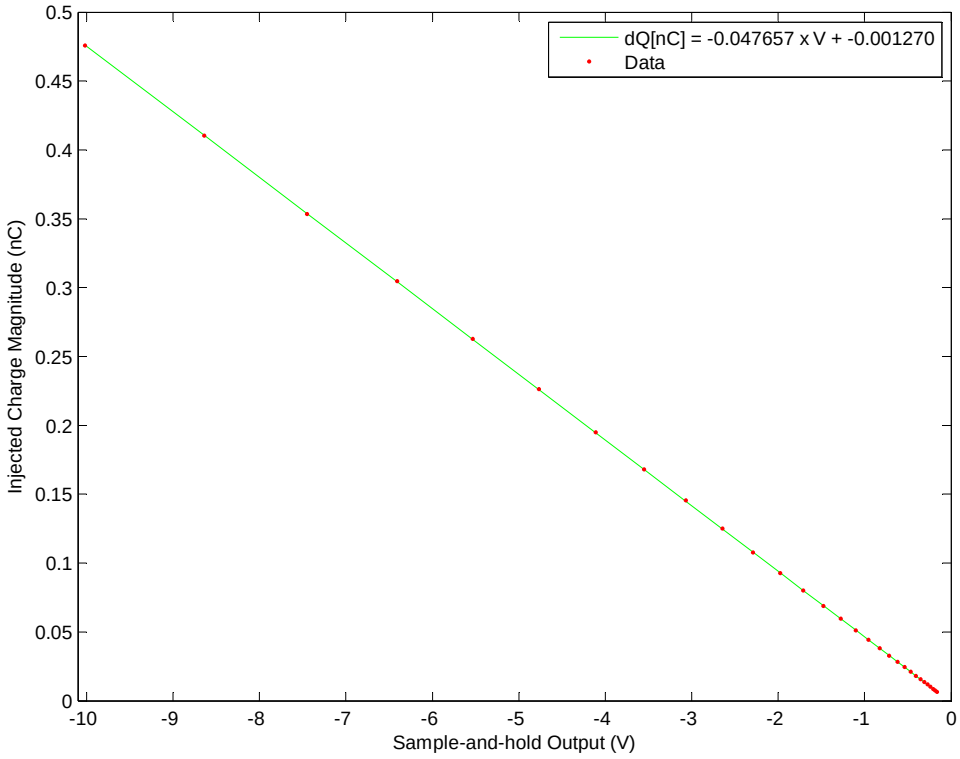

Figure 3.3: Relationship between charge injected into the circuit and output voltage of the sample-and-hold circuit. Notice the offset as compared with the previous figure, due to charge injected from the hold switch. The slope remains approximately the same.

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Appendix A

Calibration Data

The following tables show calibration values. The values $V1_{out}$, $V2_{out}$, and $V3_{out}$ are indicated in Figure 3.1. Table A.1 contains values obtained during initial design of a breadboarded circuit. The remaining tables are for the final completed circuits.

Table A.1: Initial Characterization

Input Voltage	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V3_{out}$	$V_{in}/(V1_{out}$-$V2_{out})$
0.01161	0.009419	-0.01379	0.03911	0.02532	0.5002
0.01976	0.01503	-0.02213	-0.05129	0.02916	0.5318
0.02884	0.02320	-0.03085	-0.05602	-0.02517	0.5336
0.05479	0.04867	-0.05843	-0.08441	0.02598	0.5116
0.08779	0.07417	-0.09384	-0.1233	0.02946	0.5225
0.14981	0.1200	-0.1607	-0.1894	0.02870	0.5337
0.18232	0.1504	-0.1973	-0.2225	0.0252	0.5224
0.2994	0.2418	-0.3216	-0.3511	0.0295	0.5314
0.3968	0.3257	-0.4319	-0.4588	0.0239	0.5236
0.4712	0.3867	-0.5080	-0.5415	0.0335	0.5267
0.5973	0.4904	-0.6513	-0.6823	0.0310	0.5232
0.6954	0.5715	-0.7546	-0.7830	0.0284	0.5244
0.7410	0.6088	-0.8067	-0.8412	0.0345	0.5235
0.8371	0.6889	-0.9040	-0.9390	0.0350	0.5255
0.9571	0.7847	-1.034	-1.075	0.0410	0.5263
1.0494	0.8635	-1.138	-1.176	0.038	0.5243

Table A.2: Final Calibration - Integrator 0

Input Voltage	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.039959	0.072372	-0.064790	-0.087518	-0.137163	-0.159890	-0.291327
0.046742	0.082750	-0.075444	-0.099254	-0.158194	-0.182005	-0.295471
0.053773	0.093635	-0.089293	-0.112154	-0.182928	-0.205788	-0.293958
0.063077	0.109100	-0.102752	-0.125266	-0.211852	-0.234366	-0.297741
0.073358	0.125257	-0.119371	-0.142605	-0.244629	-0.267862	-0.299873
0.085218	0.144309	-0.139338	-0.162931	-0.283647	-0.307240	-0.300438
0.098482	0.166748	-0.162087	-0.185769	-0.328835	-0.352517	-0.299487
0.114284	0.192183	-0.188854	-0.213046	-0.381037	-0.405229	-0.299930
0.132084	0.222412	-0.219616	-0.243652	-0.442028	-0.466064	-0.298815
0.153809	0.256814	-0.255393	-0.279674	-0.512207	-0.536488	-0.300286
0.177939	0.297341	-0.296897	-0.321089	-0.594238	-0.618430	-0.299440
0.206765	0.343750	-0.345747	-0.370561	-0.689497	-0.714311	-0.299878
0.240412	0.396928	-0.401278	-0.426980	-0.798207	-0.823908	-0.301190
0.278604	0.458185	-0.467862	-0.494851	-0.926048	-0.953036	-0.300853
0.323198	0.531339	-0.543590	-0.570490	-1.074929	-1.101829	-0.300669
0.375577	0.616033	-0.630416	-0.658558	-1.246449	-1.274592	-0.301318
0.434792	0.713601	-0.731623	-0.760742	-1.445224	-1.474343	-0.300848
0.506370	0.823864	-0.854270	-0.882235	-1.678134	-1.706099	-0.301746
0.585072	0.951483	-0.993652	-1.022061	-1.945135	-1.973544	-0.300787
0.680464	1.096635	-1.159224	-1.190518	-2.255859	-2.287153	-0.301643
0.791548	1.264426	-1.349432	-1.377841	-2.613858	-2.642267	-0.302828
0.919434	1.461293	-1.570268	-1.601784	-3.031561	-3.063077	-0.303287
1.062322	1.690341	-1.825506	-1.857910	-3.515847	-3.548251	-0.302153
1.232377	1.956676	-2.121804	-2.150879	-4.078480	-4.107555	-0.302166
1.430664	2.269176	-2.462935	-2.495339	-4.732111	-4.764515	-0.302331
1.661044	2.632280	-2.860662	-2.895952	-5.492942	-5.528232	-0.302396
1.927024	3.054199	-3.321422	-3.352051	-6.375621	-6.406250	-0.302249
2.236683	3.544034	-3.866300	-3.901811	-7.410334	-7.445845	-0.301833
2.595703	4.118874	-4.487305	-4.519265	-8.606179	-8.638139	-0.301609
3.011364	4.902344	-5.081676	-5.114968	-9.984020	-10.017312	-0.301618

Table A.3: Final Calibration - Integrator 1

Input Voltage	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.040847	0.065696	-0.069070	-0.095259	-0.134766	-0.160955	-0.303096
0.046697	0.076918	-0.078285	-0.104847	-0.155202	-0.181765	-0.300881
0.054075	0.088192	-0.090554	-0.118066	-0.178746	-0.206259	-0.302523
0.062314	0.102193	-0.104732	-0.131419	-0.206925	-0.233612	-0.301141
0.073162	0.118262	-0.121325	-0.147985	-0.239586	-0.266246	-0.305369
0.084375	0.137052	-0.140692	-0.167769	-0.277743	-0.304821	-0.303788
0.098686	0.158292	-0.162864	-0.189941	-0.321156	-0.348233	-0.307284
0.114311	0.183549	-0.188277	-0.215643	-0.371826	-0.399192	-0.307432
0.132484	0.212624	-0.217951	-0.245916	-0.430575	-0.458541	-0.307691
0.153587	0.246294	-0.252908	-0.281228	-0.499201	-0.527521	-0.307665
0.178161	0.285578	-0.293169	-0.321200	-0.578746	-0.606778	-0.307839
0.207280	0.330833	-0.340776	-0.369496	-0.671609	-0.700328	-0.308632
0.240190	0.383789	-0.394531	-0.424494	-0.778320	-0.808283	-0.308600
0.278311	0.442028	-0.460582	-0.491300	-0.902610	-0.933327	-0.308341
0.324050	0.513228	-0.533114	-0.563121	-1.046342	-1.076349	-0.309698
0.375488	0.596058	-0.618874	-0.648260	-1.214933	-1.244318	-0.309061
0.434770	0.692472	-0.717241	-0.747692	-1.409712	-1.440163	-0.308410
0.506658	0.798340	-0.835405	-0.867365	-1.633745	-1.665705	-0.310121
0.585849	0.922852	-0.971458	-1.004750	-1.894309	-1.927602	-0.309268
0.678400	1.064675	-1.133256	-1.165439	-2.197931	-2.230114	-0.308654
0.788952	1.227583	-1.319469	-1.351429	-2.547052	-2.579012	-0.309751
0.919434	1.416681	-1.534313	-1.570046	-2.950994	-2.986727	-0.311567
1.062633	1.638627	-1.783336	-1.818182	-3.421963	-3.456809	-0.310533
1.230735	1.902077	-2.071422	-2.104936	-3.973499	-4.007013	-0.309736
1.429909	2.206143	-2.403010	-2.434748	-4.609153	-4.640891	-0.310232
1.659668	2.561923	-2.788530	-2.817605	-5.350453	-5.379528	-0.310192
1.926048	2.971413	-3.243075	-3.274592	-6.214488	-6.246005	-0.309929
2.236594	3.457031	-3.764205	-3.801048	-7.221236	-7.258079	-0.309725
2.595526	4.018555	-4.363903	-4.399414	-8.382458	-8.417969	-0.309638
3.010920	4.771839	-4.951616	-4.980913	-9.723455	-9.752752	-0.309655

Table A.4: Final Calibration - Integrator 2

V_{in}	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.039826	0.073091	-0.063876	-0.086133	-0.136967	-0.159224	-0.290770
0.046555	0.083256	-0.074316	-0.096786	-0.157573	-0.180043	-0.295453
0.054261	0.095197	-0.087074	-0.109668	-0.182271	-0.204865	-0.297696
0.062917	0.109189	-0.101927	-0.125941	-0.211115	-0.235130	-0.298023
0.072976	0.126447	-0.118519	-0.141415	-0.244966	-0.267862	-0.297902
0.084446	0.147061	-0.137296	-0.160955	-0.284357	-0.308017	-0.296972
0.098349	0.167725	-0.160844	-0.184681	-0.328569	-0.352406	-0.299324
0.114098	0.193626	-0.186657	-0.210871	-0.380282	-0.404497	-0.300035
0.132395	0.223522	-0.217330	-0.241211	-0.440851	-0.464733	-0.300317
0.153880	0.257946	-0.252730	-0.276633	-0.510676	-0.534579	-0.301326
0.178391	0.297807	-0.294278	-0.318182	-0.592085	-0.615989	-0.301293
0.207342	0.344549	-0.343040	-0.368519	-0.687589	-0.713068	-0.301549
0.239995	0.399103	-0.399858	-0.424583	-0.798961	-0.823686	-0.300383
0.278578	0.460760	-0.464311	-0.490678	-0.925071	-0.951438	-0.301142
0.323340	0.532582	-0.539329	-0.565430	-1.071911	-1.098011	-0.301648
0.374800	0.618164	-0.626421	-0.653320	-1.244585	-1.271484	-0.301145
0.435214	0.715021	-0.727361	-0.754439	-1.442383	-1.469460	-0.301733
0.505238	0.824751	-0.850497	-0.878019	-1.675249	-1.702770	-0.301590
0.585605	0.952814	-0.987660	-1.017401	-1.940474	-1.970215	-0.301784
0.680376	1.099299	-1.153232	-1.181419	-2.252531	-2.280718	-0.302049
0.790106	1.267756	-1.343439	-1.371626	-2.611195	-2.639382	-0.302584
0.918990	1.463956	-1.564276	-1.594016	-3.028232	-3.057972	-0.303474
1.063876	1.690119	-1.817516	-1.847479	-3.507635	-3.537598	-0.303303
1.230957	1.958008	-2.113592	-2.142445	-4.071600	-4.100453	-0.302328
1.429865	2.269398	-2.456277	-2.488459	-4.725675	-4.757857	-0.302574
1.660334	2.631836	-2.851562	-2.882413	-5.483398	-5.514249	-0.302793
1.926669	3.050426	-3.317205	-3.344727	-6.367631	-6.395153	-0.302572
2.236950	3.547141	-3.852539	-3.887607	-7.399680	-7.434748	-0.302304
2.595703	4.121982	-4.471768	-4.499734	-8.593750	-8.621716	-0.302045
3.010920	5.062145	-4.894798	-4.920099	-9.956943	-9.982244	-0.302394

Table A.5: Final Calibration - Integrator 3

V_{in}	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.039933	0.061328	-0.076571	-0.101412	-0.137900	-0.162740	-0.289577
0.046351	0.072781	-0.087402	-0.111115	-0.160183	-0.183896	-0.289364
0.054039	0.084872	-0.099938	-0.124840	-0.184810	-0.209712	-0.292405
0.062651	0.099165	-0.114968	-0.139151	-0.214133	-0.238317	-0.292579
0.073011	0.116087	-0.131827	-0.156401	-0.247914	-0.272487	-0.294503
0.084668	0.135032	-0.151634	-0.177313	-0.286666	-0.312345	-0.295355
0.097834	0.157448	-0.176225	-0.201616	-0.333674	-0.359064	-0.293202
0.114205	0.184104	-0.201771	-0.227117	-0.385875	-0.411222	-0.295962
0.132679	0.213934	-0.232200	-0.258434	-0.446134	-0.472368	-0.297398
0.153223	0.249334	-0.268399	-0.293967	-0.517734	-0.543302	-0.295949
0.178214	0.290350	-0.310658	-0.336248	-0.601008	-0.626598	-0.296525
0.206996	0.337180	-0.359775	-0.386008	-0.696955	-0.723189	-0.297000
0.240288	0.392489	-0.415527	-0.442916	-0.808017	-0.835405	-0.297380
0.278951	0.454901	-0.482688	-0.510565	-0.937589	-0.965465	-0.297519
0.323517	0.527521	-0.559215	-0.587535	-1.086737	-1.115057	-0.297696
0.375266	0.614258	-0.646840	-0.674805	-1.261097	-1.289063	-0.297571
0.435059	0.713601	-0.748224	-0.778231	-1.461825	-1.491832	-0.297613
0.504838	0.828835	-0.868164	-0.897550	-1.696999	-1.726385	-0.297489
0.585716	0.957697	-1.009854	-1.042037	-1.967551	-1.999734	-0.297688
0.681552	1.108176	-1.176758	-1.206942	-2.284934	-2.315118	-0.298281
0.790039	1.279519	-1.369629	-1.403587	-2.649148	-2.683106	-0.298224
0.915705	1.479048	-1.591797	-1.624423	-3.070845	-3.103471	-0.298193
1.063477	1.706543	-1.850586	-1.882324	-3.557129	-3.588867	-0.298971
1.233975	1.977095	-2.149325	-2.181064	-4.126420	-4.158159	-0.299043
1.431552	2.294922	-2.492898	-2.528187	-4.787820	-4.823109	-0.298999
1.659890	2.664684	-2.891513	-2.926802	-5.556197	-5.591486	-0.298746
1.925515	3.093040	-3.361594	-3.390891	-6.454634	-6.483931	-0.298315
2.236861	3.601740	-3.899148	-3.930220	-7.500888	-7.531960	-0.298213
2.595881	4.196999	-4.519265	-4.545455	-8.716264	-8.742454	-0.297820
3.010476	5.059482	-5.049716	-5.084339	-10.109198	-10.143821	-0.297796

Table A.6: Final Calibration - Integrator 4

V_{in}	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.040359	0.072310	-0.062180	-0.084748	-0.134490	-0.157058	-0.300086
0.046591	0.082910	-0.073100	-0.094913	-0.156010	-0.177823	-0.298640
0.054066	0.095508	-0.084570	-0.107449	-0.180078	-0.202956	-0.300237
0.063015	0.109535	-0.099450	-0.121884	-0.208984	-0.231419	-0.301529
0.073207	0.126358	-0.116291	-0.138423	-0.242649	-0.264782	-0.301698
0.084695	0.144820	-0.135542	-0.158181	-0.280362	-0.303001	-0.302090
0.098304	0.166792	-0.157582	-0.182373	-0.324374	-0.349165	-0.303059
0.113725	0.192693	-0.183616	-0.206388	-0.376309	-0.399081	-0.302212
0.132946	0.221080	-0.213778	-0.236772	-0.434859	-0.457852	-0.305722
0.153445	0.255704	-0.248846	-0.272772	-0.504550	-0.528476	-0.304122
0.178187	0.295699	-0.289573	-0.313721	-0.585272	-0.609419	-0.304452
0.206863	0.340909	-0.337535	-0.362393	-0.678445	-0.703303	-0.304907
0.240368	0.393954	-0.393244	-0.417037	-0.787198	-0.810991	-0.305346
0.278551	0.454457	-0.457475	-0.482777	-0.911932	-0.937234	-0.305452
0.323420	0.526367	-0.531694	-0.556463	-1.058061	-1.082830	-0.305672
0.375511	0.609996	-0.617365	-0.644354	-1.227362	-1.254350	-0.305949
0.435303	0.705788	-0.716797	-0.742898	-1.422585	-1.448686	-0.305994
0.505149	0.814320	-0.837846	-0.864924	-1.652166	-1.679244	-0.305750
0.585161	0.940829	-0.973455	-1.002974	-1.914284	-1.943803	-0.305681
0.680908	1.083540	-1.136808	-1.164551	-2.220348	-2.248091	-0.306667
0.791593	1.248446	-1.325018	-1.351651	-2.573464	-2.600097	-0.307598
0.917924	1.443537	-1.540305	-1.569824	-2.983842	-3.013361	-0.307632
1.063255	1.667924	-1.792658	-1.823952	-3.460582	-3.491876	-0.307247
1.231357	1.932706	-2.083185	-2.112038	-4.015891	-4.044744	-0.306621
1.428400	2.242321	-2.419434	-2.453613	-4.661755	-4.695934	-0.306408
1.660467	2.600985	-2.809171	-2.841797	-5.410156	-5.442782	-0.306917
1.926136	3.016246	-3.267489	-3.300337	-6.283735	-6.316583	-0.306527
2.236683	3.509854	-3.796609	-3.831676	-7.306463	-7.341530	-0.306124
2.595703	4.080256	-4.404741	-4.438033	-8.484997	-8.518289	-0.305917
3.010565	5.083008	-4.750089	-4.781161	-9.833097	-9.864169	-0.306167

Table A.7: Final Calibration - Integrator 5

V_{in}	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.040288	0.073100	-0.065128	-0.090838	-0.138228	-0.163938	-0.291458
0.046156	0.084011	-0.076252	-0.102175	-0.160263	-0.186186	-0.288001
0.054128	0.096609	-0.088947	-0.114693	-0.185556	-0.211301	-0.291709
0.062571	0.111772	-0.103693	-0.129332	-0.215465	-0.241104	-0.290400
0.072931	0.127557	-0.121520	-0.147488	-0.249077	-0.275044	-0.292807
0.084419	0.147860	-0.141091	-0.166837	-0.288952	-0.314697	-0.292158
0.098642	0.170277	-0.164351	-0.189875	-0.334628	-0.360152	-0.294780
0.114276	0.196689	-0.191184	-0.217374	-0.387873	-0.414063	-0.294621
0.131827	0.227361	-0.221879	-0.247780	-0.449241	-0.475142	-0.293444
0.153516	0.262451	-0.258501	-0.285778	-0.520952	-0.548229	-0.294683
0.178436	0.303245	-0.299916	-0.327681	-0.603161	-0.630926	-0.295834
0.206898	0.350630	-0.349609	-0.377086	-0.700240	-0.727717	-0.295468
0.240190	0.405140	-0.405540	-0.433461	-0.810680	-0.838601	-0.296282
0.278702	0.468040	-0.472745	-0.501243	-0.940785	-0.969283	-0.296244
0.323606	0.542347	-0.549095	-0.579190	-1.091442	-1.121538	-0.296494
0.375089	0.628906	-0.638317	-0.668945	-1.267223	-1.297851	-0.295993
0.434748	0.728338	-0.741033	-0.772550	-1.469371	-1.500888	-0.295873
0.505549	0.839622	-0.866033	-0.898216	-1.705655	-1.737837	-0.296396
0.584717	0.971014	-1.004750	-1.038263	-1.975764	-2.009277	-0.295945
0.680642	1.120384	-1.174094	-1.207608	-2.294478	-2.327992	-0.296643
0.789706	1.290838	-1.368741	-1.400479	-2.659579	-2.691317	-0.296929
0.917591	1.489924	-1.592019	-1.622869	-3.081943	-3.112793	-0.297731
1.063565	1.720082	-1.851474	-1.882990	-3.571556	-3.603072	-0.297788
1.232644	1.991966	-2.152433	-2.185059	-4.144399	-4.177025	-0.297424
1.429643	2.310458	-2.499334	-2.531960	-4.809792	-4.842418	-0.297236
1.660334	2.680220	-2.902832	-2.935902	-5.583052	-5.616122	-0.297388
1.924450	3.105913	-3.377131	-3.410423	-6.483044	-6.516336	-0.296844
2.236506	3.612393	-3.924006	-3.954190	-7.536399	-7.566583	-0.296761
2.595881	4.198331	-4.549893	-4.585849	-8.748224	-8.784180	-0.296732
3.010298	5.408381	-4.722567	-4.751864	-10.130948	-10.160245	-0.297139

Table A.8: Final Calibration - Integrator 6

V_{in}	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.039933	0.070472	-0.066371	-0.087864	-0.136843	-0.158336	-0.291813
0.046600	0.080549	-0.076287	-0.099272	-0.156836	-0.179821	-0.297124
0.054110	0.092969	-0.088965	-0.111222	-0.181934	-0.204190	-0.297419
0.062802	0.106774	-0.104412	-0.126562	-0.211186	-0.233336	-0.297377
0.072905	0.124112	-0.120827	-0.143359	-0.244940	-0.267472	-0.297644
0.084837	0.142800	-0.140092	-0.162576	-0.282892	-0.305376	-0.299890
0.098340	0.165017	-0.163197	-0.185236	-0.328214	-0.350253	-0.299621
0.114338	0.190896	-0.189054	-0.210827	-0.379949	-0.401722	-0.300929
0.132147	0.221280	-0.219860	-0.243009	-0.441140	-0.464289	-0.299557
0.153720	0.255704	-0.255438	-0.278675	-0.511142	-0.534379	-0.300738
0.177512	0.295898	-0.296165	-0.319336	-0.592063	-0.615234	-0.299820
0.206996	0.342552	-0.344505	-0.369229	-0.687056	-0.711781	-0.301279
0.239711	0.395819	-0.400169	-0.424893	-0.795987	-0.820712	-0.301149
0.278720	0.457298	-0.465732	-0.490057	-0.923029	-0.947354	-0.301962
0.322816	0.530096	-0.541193	-0.565785	-1.071289	-1.095881	-0.301334
0.375155	0.615057	-0.628374	-0.653675	-1.243430	-1.268732	-0.301710
0.435525	0.712447	-0.728604	-0.754972	-1.441051	-1.467418	-0.302227
0.505016	0.826261	-0.846413	-0.873491	-1.672674	-1.699752	-0.301921
0.584717	0.952370	-0.988992	-1.017401	-1.941362	-1.969771	-0.301189
0.681330	1.099964	-1.153010	-1.182306	-2.252974	-2.282270	-0.302414
0.790794	1.266424	-1.342995	-1.371626	-2.609419	-2.638050	-0.303054
0.918368	1.460849	-1.563832	-1.593794	-3.024681	-3.054643	-0.303625
1.062678	1.687012	-1.818626	-1.847257	-3.505638	-3.534269	-0.303134
1.233709	1.953791	-2.114036	-2.144221	-4.067827	-4.098012	-0.303285
1.428533	2.265847	-2.454723	-2.478471	-4.720570	-4.744318	-0.302619
1.658869	2.628951	-2.850453	-2.879306	-5.479404	-5.508257	-0.302746
1.925515	3.048651	-3.315430	-3.345170	-6.364081	-6.393821	-0.302560
2.236950	3.544478	-3.848544	-3.876065	-7.393022	-7.420543	-0.302576
2.595792	4.122869	-4.461115	-4.489524	-8.583984	-8.612393	-0.302399
3.011630	5.076793	-4.865501	-4.896129	-9.942294	-9.972922	-0.302911

Table A.9: Final Calibration - Integrator 7

V_{in}	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.039862	0.071271	-0.067445	-0.093271	-0.138716	-0.164542	-0.287360
0.046165	0.080415	-0.079039	-0.104199	-0.159455	-0.184615	-0.289516
0.053418	0.094070	-0.090687	-0.115030	-0.184757	-0.209100	-0.289126
0.062669	0.108816	-0.105291	-0.130566	-0.214107	-0.239382	-0.292698
0.073065	0.125364	-0.123003	-0.148136	-0.248366	-0.273500	-0.294181
0.084837	0.144398	-0.142955	-0.167747	-0.287354	-0.312145	-0.295234
0.098491	0.167458	-0.166482	-0.191628	-0.333940	-0.359086	-0.294936
0.114169	0.193759	-0.193515	-0.218572	-0.387274	-0.412331	-0.294802
0.132484	0.223877	-0.224521	-0.249490	-0.448398	-0.473367	-0.295461
0.153560	0.258944	-0.259766	-0.285489	-0.518710	-0.544434	-0.296042
0.178116	0.299849	-0.301292	-0.325817	-0.601141	-0.625666	-0.296297
0.206632	0.347301	-0.351207	-0.377974	-0.698508	-0.725275	-0.295818
0.240412	0.401989	-0.407804	-0.435059	-0.809792	-0.837047	-0.296881
0.278471	0.464844	-0.474521	-0.502220	-0.939364	-0.967063	-0.296446
0.323651	0.538441	-0.550959	-0.579190	-1.089400	-1.117631	-0.297091
0.375244	0.625621	-0.638672	-0.668945	-1.264293	-1.294567	-0.296801
0.435214	0.723722	-0.742099	-0.771928	-1.465820	-1.495650	-0.296908
0.505637	0.836293	-0.865811	-0.895552	-1.702104	-1.731845	-0.297066
0.585161	0.967685	-1.006081	-1.038042	-1.973766	-2.005727	-0.296469
0.680353	1.117942	-1.173873	-1.205167	-2.291815	-2.323109	-0.296862
0.789551	1.286621	-1.366522	-1.398038	-2.653143	-2.684659	-0.297591
0.918413	1.484375	-1.591131	-1.621316	-3.075506	-3.105691	-0.298622
1.065075	1.713867	-1.851030	-1.882102	-3.564897	-3.595969	-0.298767
1.234375	1.982644	-2.151767	-2.182395	-4.134411	-4.165039	-0.298561
1.432884	2.302912	-2.496893	-2.529297	-4.799805	-4.832209	-0.298530
1.660245	2.672008	-2.897949	-2.925249	-5.569957	-5.597257	-0.298071
1.926669	3.097923	-3.370916	-3.403320	-6.468839	-6.501243	-0.297838
2.237038	3.604847	-3.912021	-3.944425	-7.516868	-7.549272	-0.297602
2.595881	4.193004	-4.532138	-4.559215	-8.725142	-8.752219	-0.297517
3.010387	5.176669	-4.928533	-4.965820	-10.105202	-10.142489	-0.297905

Table A.10: Final Calibration - Integrator 8

V_{in}	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.039995	0.072319	-0.067489	-0.090172	-0.139808	-0.162491	-0.286068
0.046502	0.083301	-0.079031	-0.099787	-0.162331	-0.183088	-0.286464
0.053995	0.095703	-0.091566	-0.113929	-0.187269	-0.209632	-0.288328
0.062873	0.110378	-0.106250	-0.128001	-0.216628	-0.238379	-0.290234
0.072931	0.128063	-0.122923	-0.145987	-0.250986	-0.274050	-0.290580
0.084641	0.147017	-0.144975	-0.166770	-0.291992	-0.313787	-0.289875
0.098331	0.170965	-0.167503	-0.191140	-0.338468	-0.362105	-0.290518
0.114036	0.195779	-0.196333	-0.218839	-0.392112	-0.414617	-0.290825
0.132431	0.228005	-0.225719	-0.249157	-0.453724	-0.477162	-0.291875
0.153285	0.263317	-0.262385	-0.285822	-0.525701	-0.549139	-0.291581
0.178383	0.304088	-0.304887	-0.327748	-0.608976	-0.631836	-0.292922
0.206836	0.353072	-0.354892	-0.378285	-0.707963	-0.731356	-0.292156
0.240749	0.407626	-0.412243	-0.436523	-0.819869	-0.844150	-0.293644
0.278888	0.471413	-0.480202	-0.505682	-0.951616	-0.977095	-0.293068
0.323375	0.546165	-0.557084	-0.582031	-1.103249	-1.128196	-0.293112
0.375155	0.634322	-0.646662	-0.671697	-1.280984	-1.306019	-0.292865
0.434637	0.734553	-0.750000	-0.774858	-1.484553	-1.509411	-0.292773
0.505083	0.848500	-0.875799	-0.902655	-1.724299	-1.751154	-0.292921
0.586803	0.979448	-1.017401	-1.044478	-1.996849	-2.023926	-0.293865
0.683327	1.131481	-1.186301	-1.216486	-2.317782	-2.347967	-0.294820
0.787931	1.300604	-1.384055	-1.412243	-2.684659	-2.712847	-0.293494
0.914529	1.500355	-1.611994	-1.640625	-3.112349	-3.140980	-0.293839
1.065430	1.733176	-1.874778	-1.904519	-3.607954	-3.637695	-0.295300
1.235174	2.011497	-2.175071	-2.202370	-4.186568	-4.213867	-0.295033
1.434881	2.332653	-2.528187	-2.558594	-4.860840	-4.891247	-0.295192
1.661621	2.707076	-2.934126	-2.963867	-5.641202	-5.670943	-0.294551
1.925160	3.138761	-3.411310	-3.437056	-6.550071	-6.575817	-0.293914
2.237482	3.651456	-3.961737	-3.989258	-7.613193	-7.640714	-0.293895
2.595792	4.244052	-4.592951	-4.621360	-8.837003	-8.865412	-0.293741
3.010831	5.082564	-5.162464	-5.184659	-10.245028	-10.267223	-0.293882

Table A.11: Final Calibration - Integrator 9

V_{in}	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.040297	0.069602	-0.065376	-0.090217	-0.134979	-0.159819	-0.298540
0.046795	0.080185	-0.075906	-0.099574	-0.156090	-0.179759	-0.299795
0.054403	0.092330	-0.088503	-0.112944	-0.180833	-0.205273	-0.300849
0.062562	0.107449	-0.102885	-0.126500	-0.210334	-0.233949	-0.297442
0.073544	0.123091	-0.119753	-0.143706	-0.242845	-0.266797	-0.302844
0.084677	0.142512	-0.139360	-0.164329	-0.281871	-0.306840	-0.300410
0.098118	0.164972	-0.161621	-0.186812	-0.326594	-0.351785	-0.300428
0.113832	0.189253	-0.188565	-0.213645	-0.377819	-0.402899	-0.301287
0.132653	0.220037	-0.218151	-0.243164	-0.438188	-0.463201	-0.302730
0.153516	0.254483	-0.253285	-0.280229	-0.507768	-0.534712	-0.302334
0.178223	0.294079	-0.294167	-0.319536	-0.588246	-0.613614	-0.302973
0.207209	0.340288	-0.343306	-0.370162	-0.683594	-0.710449	-0.303117
0.240146	0.393910	-0.398304	-0.424139	-0.792214	-0.818049	-0.303132
0.278684	0.454989	-0.463512	-0.491389	-0.918501	-0.946378	-0.303412
0.323642	0.526633	-0.538352	-0.565785	-1.064986	-1.092418	-0.303893
0.375466	0.611417	-0.624645	-0.653675	-1.236062	-1.265092	-0.303760
0.434637	0.708896	-0.724965	-0.754350	-1.433860	-1.463246	-0.303124
0.505859	0.818537	-0.846280	-0.876909	-1.664817	-1.695446	-0.303853
0.586648	0.946378	-0.983221	-1.014515	-1.929599	-1.960893	-0.304026
0.679776	1.091531	-1.146573	-1.177424	-2.238104	-2.268955	-0.303729
0.787931	1.256658	-1.336559	-1.367409	-2.593217	-2.624067	-0.303843
0.919123	1.450195	-1.555620	-1.586914	-3.005815	-3.037109	-0.305782
1.063255	1.676358	-1.808638	-1.839267	-3.484996	-3.515625	-0.305095
1.233132	1.941806	-2.102051	-2.134455	-4.043857	-4.076261	-0.304940
1.428356	2.253862	-2.439853	-2.472479	-4.693715	-4.726341	-0.304312
1.658514	2.613858	-2.831809	-2.862438	-5.445667	-5.476296	-0.304557
1.925870	3.031339	-3.293679	-3.324308	-6.325018	-6.355647	-0.304485
2.237660	3.523615	-3.825906	-3.856978	-7.349521	-7.380593	-0.304463
2.596147	4.098011	-4.437589	-4.460671	-8.535600	-8.558682	-0.304155
3.011896	4.877930	-5.023526	-5.056818	-9.901456	-9.934748	-0.304187

Table A.12: Final Calibration - Integrator A

V_{in}	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.040314	0.071839	-0.066877	-0.088308	-0.138716	-0.160147	-0.290624
0.046573	0.082724	-0.077406	-0.099920	-0.160130	-0.182644	-0.290847
0.054466	0.095384	-0.090234	-0.112527	-0.185618	-0.207910	-0.293428
0.063290	0.109881	-0.105229	-0.127122	-0.215110	-0.237003	-0.294222
0.072878	0.127512	-0.122221	-0.145082	-0.249734	-0.272594	-0.291824
0.084908	0.146951	-0.142156	-0.164950	-0.289107	-0.311901	-0.293690
0.098233	0.169434	-0.165816	-0.188898	-0.335249	-0.358332	-0.293016
0.113725	0.195956	-0.192605	-0.214466	-0.388561	-0.410423	-0.292683
0.132253	0.226119	-0.223522	-0.246649	-0.449640	-0.472767	-0.294131
0.153285	0.261652	-0.259455	-0.283758	-0.521107	-0.545410	-0.294152
0.177823	0.302623	-0.301913	-0.325417	-0.604537	-0.628041	-0.294148
0.207031	0.349965	-0.351740	-0.376598	-0.701705	-0.726563	-0.295040
0.240403	0.404963	-0.408203	-0.433061	-0.813166	-0.838024	-0.295638
0.278507	0.466708	-0.476385	-0.502308	-0.943093	-0.969016	-0.295312
0.322914	0.541726	-0.552291	-0.577770	-1.094016	-1.119496	-0.295163
0.374956	0.628995	-0.640536	-0.665660	-1.269531	-1.294656	-0.295350
0.434970	0.727983	-0.744229	-0.771307	-1.472212	-1.499290	-0.295453
0.505637	0.839844	-0.868253	-0.896662	-1.708096	-1.736506	-0.296024
0.584584	0.970348	-1.009854	-1.037598	-1.980202	-2.007946	-0.295214
0.680131	1.119274	-1.178977	-1.208718	-2.298251	-2.327992	-0.295934
0.788929	1.288397	-1.374068	-1.402921	-2.662465	-2.691318	-0.296315
0.917591	1.485929	-1.599565	-1.627530	-3.085494	-3.113459	-0.297389
1.065385	1.717640	-1.860352	-1.889870	-3.577992	-3.607510	-0.297761
1.235795	1.991966	-2.161754	-2.190607	-4.153720	-4.182573	-0.297515
1.432306	2.309348	-2.510210	-2.537065	-4.819558	-4.846413	-0.297186
1.661000	2.678001	-2.915705	-2.943226	-5.593706	-5.621227	-0.296941
1.924893	3.105469	-3.389116	-3.413530	-6.494585	-6.518999	-0.296384
2.236861	3.611506	-3.936879	-3.963068	-7.548385	-7.574574	-0.296336
2.595614	4.197443	-4.563210	-4.595170	-8.760653	-8.792613	-0.296281
3.010387	5.205522	-4.940518	-4.972035	-10.146040	-10.177557	-0.296706

Table A.13: Final Calibration - Integrator B

V_{in}	$V1_{out}$	$V2_{out}$	$V3_{out}$	$V2_{out}$-$V1_{out}$	$V3_{out}$-$V1_{out}$	$V_{in}/(V2_{out}$-$V1_{out})$
0.040243	0.060964	-0.072985	-0.096165	-0.133949	-0.157129	-0.300437
0.046502	0.071538	-0.083736	-0.108425	-0.155273	-0.179963	-0.299485
0.054004	0.083789	-0.095206	-0.118945	-0.178995	-0.202734	-0.301706
0.062571	0.097665	-0.110334	-0.133967	-0.207999	-0.231632	-0.300824
0.073038	0.114027	-0.126829	-0.150675	-0.240856	-0.264702	-0.303244
0.084854	0.132480	-0.146396	-0.170233	-0.278875	-0.302712	-0.304274
0.098047	0.154208	-0.168990	-0.193293	-0.323198	-0.347501	-0.303365
0.114347	0.180065	-0.194780	-0.219371	-0.374845	-0.399436	-0.305051
0.132395	0.209606	-0.225253	-0.249734	-0.434859	-0.459340	-0.304456
0.153835	0.243075	-0.260298	-0.285067	-0.503374	-0.528143	-0.305608
0.178240	0.283425	-0.300670	-0.325417	-0.584095	-0.608842	-0.305156
0.206960	0.329590	-0.348810	-0.374334	-0.678400	-0.703924	-0.305071
0.239932	0.383212	-0.403143	-0.427956	-0.786355	-0.811168	-0.305120
0.278764	0.444336	-0.466886	-0.493430	-0.911222	-0.937766	-0.305924
0.323269	0.512873	-0.543413	-0.569869	-1.056286	-1.082742	-0.306043
0.375422	0.598633	-0.627575	-0.655895	-1.226207	-1.254528	-0.306165
0.434992	0.694869	-0.727095	-0.755682	-1.421964	-1.450550	-0.305909
0.504572	0.806996	-0.843129	-0.871271	-1.650124	-1.678267	-0.305778
0.585338	0.932839	-0.982999	-1.012518	-1.915838	-1.945357	-0.305526
0.681108	1.078880	-1.145463	-1.175204	-2.224343	-2.254084	-0.306206
0.789751	1.244007	-1.331676	-1.363858	-2.575683	-2.607865	-0.306618
0.916482	1.434215	-1.550515	-1.580922	-2.984730	-3.015137	-0.307057
1.063121	1.657049	-1.801314	-1.829945	-3.458363	-3.486994	-0.307406
1.234020	1.918501	-2.092285	-2.120694	-4.010786	-4.039195	-0.307675
1.430664	2.227450	-2.429865	-2.462269	-4.657315	-4.689719	-0.307186
1.660201	2.585005	-2.818049	-2.847346	-5.403054	-5.432351	-0.307271
1.925959	2.999822	-3.277255	-3.306552	-6.277077	-6.306374	-0.306824
2.236772	3.493430	-3.801048	-3.825018	-7.294478	-7.318448	-0.306639
2.596946	4.072266	-4.405185	-4.440696	-8.477451	-8.512962	-0.306336
3.010653	4.883700	-4.924982	-4.957386	-9.808682	-9.841086	-0.306938