Patterning Vertical Structures for Use in Constructing Amorphous Silicon Solar Cell Molds

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Abstract

The purpose of the capstone project was to develop a less costly process of patterning vertical structures in amorphous silicon for use in photovoltaics. Two processes were followed in trying to develop the mold. The first process centered on using a 3 micron layer of photoresist SU-8 10, a viscous polymer creating a pattern using lithography and spun on hydrogen silsesquioxane (HSQ) to create a reusable reverse glass mold. This process resulted in an unusable pattern with unclean lines and definition. A second process was planned after the failure of the first process. The second process centered on polyimide, a different polymer, using lithography to create a reusable reverse mold. The initial results with polyimide are promising and will continue to be investigated.

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Chapter 1

1 Introduction

1.1 Motivation for Research

Inexpensive, clean, renewable energy is the motivation for this research. Solar energy might win a competition as the most clean and renewable energy source, but has not been able to compete with other energy groups in terms of expense. There is an existing niche market for solar energy, but this would expand on a global scale if cost could be controlled. While promotion of renewable energy may be politically correct to support, practicality requires that any widespread use of solar cells for energy production must be economical as well. Even when petroleum based energy prices reached record highs in the summer of 2008, solar energy could not compete with gas, coal, or nuclear energy in cost measured as[1] Cents/kW-h as Figure 1.1 illustrates.

Method	Cents/kW-h
Gas Currently supplies around 15% of the global electricity demand.	3.9 - 4.4 Cents/kW-h
Coal Currently supplies around 38% of the global electricity demand.	4.8 - 5.5 Cents/kW-h
Nuclear Currently supplies around 24% of the global electricity demand.	11.1 - 14.5 Cents/kW-h
Solar Currently supplies approximately 0.8% of the global electricity demand.	15 - 30 Cents/kW-h

Figure 1.1.1 Power Generation Costs[1]

Photovoltaic research is one portion of solar energy research that is being investigated as a means of creating an inexpensive alternative to other energy sources. Traditionally,

the two main focal points of photovoltaic research have been to make solar cells cheaper by using less expensive manufacturing methods with cheaper materials and to make solar cells more efficient in energy output.[2] This two pronged approach is also the basis for this research, cheaper solar cells that produce more energy.

1.2 Background of Solar Cells

The known history of photovoltaics began in 1839 when the French physicist Alexandre Edmond Becquerel discovered that illumination of light on electrodes and electrolyte increased conductance, a photovoltaic effect.[3] As with most scientific advances, Becquerel's discoveries became the building blocks of future photovoltaic research. In 1873 Willoughby Smith discovered a photovoltaic effect with selenium which, along with other selenium research, led to the construction of the first selenium solar cell, an event which was recorded by Charles Fritts in 1876.[3] Some years later, Albert Einstein described a detailed theoretical explanation of the photovoltaic effect in 1905, along with another theory on relativity. Einstein later received a Nobel Prize for his work in the area of photovoltaics in 1921.[4]

The field of photovoltaic research was inadvertently expanded in 1916 when Jan Czochralski, a Polish scientist, discovered the crystalline properties of tin because of a small mistake. His was an example of putting something in the wrong place at the right time, or maybe just a little scientific luck. Jan Czochralski was trying to dip his pen in an inkwell, but inadvertently stuck the pen in a molten container of tin. He pulled out a single string of metal and noticed it had a crystal structure.[5] It may have seemed an insignificant discovery, but it was actually of great significance. A similar process has been continually used in the creation of industrial crystals, using what has come to be

known as the 'Czochralski Method.'[5] Scientists at Bell Laboratories used the research of Czochralski to create germanium single crystals, and later silicon crystals. These were used to make the first transistor and, some time later, many of the components that supported the development of the semiconductor industry.[6] This discovery proved to have application beyond semiconductors. In 1954, using the silicon crystals developed at Bell Laboratory, three scientists, Daryl Chapin, Calvin Fuller, and Gerald Person, developed a silicon photovoltaic cell capable of running small electrical equipment.[3]

In the 1950s and 1960s, photovoltaic research and discovery grew exponentially. Many electronics companies joined in the research by developing solar cells that were used in space exploration.[3] Solar cells began to appear in the commercial market also. These commercial solar cells were expensive to produce, but a niche industry developed that provided solar energy where there was no other feasible source. During the 1970s, this limited commercial viability of photovoltaic research led many large corporations to try to produce more efficient inexpensive solar cells that could provide larger amounts of energy. The goal was to compete with commercial energy production.[4]

A less expensive method for creating solar cells was finally explained in detail in 1976 through the research of amorphous silicon (a-Si) solar cells by Carlson and Wronski. They expanded on a-Si solar cell research which had begun in the 1960s.[7] The a-Si solar cells would power items such as solar calculators. These successes led to research into different materials and production methods in an attempt to market photovoltaic cells that produced energy over a longer period of time.

The United States government joined in the research when various national laboratories began researching photovoltaic and solar related energy production. For

instance, the solar research facilities at Sandia National Laboratories (SNL) in Albuquerque, New Mexico, one of the Department of Energy's laboratories, focused on photovoltaic grids, trying to determine solar cell efficiencies over long periods of time. Other research at SNL involved alternative solar research that used reflective mirrors and a stirling salt engine in an attempt to clean polluted water.[8] In the year 2000, Sandia National Laboratories developed a new kind of inverter for solar electric systems which is capable of converting from direct current (DC) to alternating current (AC). This enables photovoltaic energy to be used by private, non-commercial parties.[9] Other Department of Energy Labs in addition to SNL are working in photovoltaic research, including the National Renewable Energy Laboratory (NREL). To direct and focus these research efforts, the U.S. government, in conjunction with private industry partners, has developed a Photovoltaic Industry Roadmap for the years 2000 to 2020.[10] The top technical barrier to greater use of solar cells that was identified in the Photovoltaic Industry Roadmap was the need to design a means to manufacture photovoltaic solar cells at a price that can compete with other energy producing industries.[11]

This is an exciting time for photovoltaic and other forms of alternative energy as the means to fund research to overcome the identified technical problems would now seem to be at hand. Dr. Steven Chu, a former director of a national laboratory, an advocate for alternate energy, a Nobel Prize winner in physics, and the recently appointed U.S. Secretary of Energy will be responsible for spending roughly 18 billion dollars of taxpayer money on clean energy over the 2009 calendar year. This funding was included in the economic stimulus package enacted in February, 2009. Some of this money is specifically earmarked for photovoltaic research.[12] Considering that the current budget

for the entire Department of Energy is 25 billion dollars a year, [12] this level of funding will be a significant government investment in solar cell research and development.

1.3 How Amorphous Silicon Solar Cells Work

Ninety-five percent of the solar cells in use today are made from the element silicon, one of the more abundant elements on the earth. Silicon is one of the more environmentally friendly products to produce and use.[13] Silicon does not normally appear as an element, but instead as silicon dioxide, or sand, which must be refined. There are three main types of silicon that are used in solar cell technology: monocrystalline silicon (c-Si), polycrystalline silicon (poly-Si), and amorphous silicon (a-Si). Monocrystalline is the most efficient, but is also the most expensive.[13] Monocrystalline silicon is made using the 'Czochralski Method' by creating a large ingot of silicon arranged in a crystal lattice. (Figure 1.3.1) Doping elements are added in the process to make the silicon sensitive to positive charge carriers or negative charge carriers, which make up the p/n junction allowing solar cells to produce energy from the sun.[13] Creating and cutting the ingots is an expensive process because up to half the ingot is lost in the cutting process. However, c-Si makes the most efficient solar cells. They can last twenty or more years.

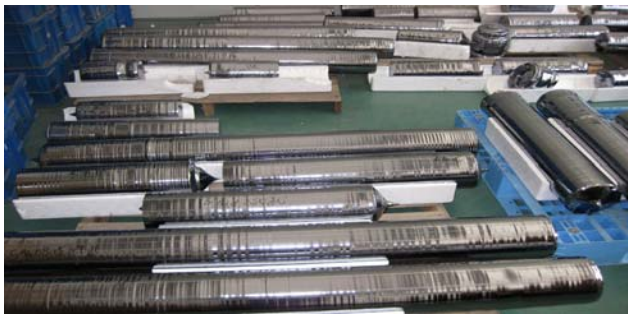


Figure 1.3.1 Monocrystalline Silicon Ingots[14]

The process to create poly-Si is not as expensive as creating c-Si, but the cutting process is still cost prohibitive. The crystalline structure is not one crystal, but many. It is also not as efficient in creating electricity as c-Si, but these cells are making inroads commercially against c-Si solar cells because of the lower production price. (Figure 1.3.2)



Figure 1.3.2 Polycrystalline Silicon Rod[15]

Amorphous silicon does not start out as ingots or rods that have to be cut, but as a gas, silane (SiH_4). It can be vapor deposited onto glass or other materials, such as plastic, to create thin films which can be used for solar cells. (Figure 1.3.3) Liquid crystal displays (LCD) are made in a similar process.

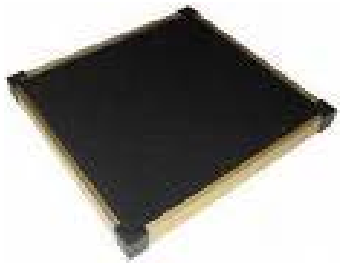


Figure 1.3.3 Amorphous Silicon Thin Cell[16]

Silicon has a four fold coordinated atom pattern that is tetrahedral in shape and can bond to four other atoms. Crystalline silicon bonds with itself, forming a lattice which gives it great strength. Amorphous silicon is not organized like crystalline silicon. It is not always four folding and can have a dangling bond. Hydrogen is sometimes added to a-Si to stabilize the material by filling the incomplete bond. This a-Si:H material can then

be used for solar cells. However, a-Si:H does have two drawbacks. The first is that light can degrade the amorphous silicon, which reduces the efficiency of the cell. This is referred to as a burning in period, called the Staebler-Wronski Effect after those who discovered it.[17] The second drawback is that a-Si:H cells are not as efficient as c-Si or poly-Si in creating power. Despite these concerns, a-Si:H is inexpensive to produce and is very cost effective.

Amorphous silicon can be deposited on large areas because it can be applied by vapor deposition. The process of chemical vapor deposition exposes the wafer (substrate) in order to decompose the substrate surface and produce the desired deposit. Processes of chemical vapor deposition differ according to how the activation of the chemical reaction is initiated. One method for distributing a-Si:H_4 is to use a plasma-enhanced chemical vapor deposition (PEVCD) machine as illustrated in Figure 1.3.4. The PECVD process uses plasma to enhance the chemical reaction rates so a lower processing temperature can be used. Silane is a good choice for an aluminum substrate since this metal is sensitive to high temperature.[18] Use of the PEVCD results in a deposit that is about 100 nanometers to 150 nanometers thick, significantly reducing the amount of Si and the processing expense. This, in turn, reduces the price of creating a solar cell.[3] The amorphous silicon is very thin, but can still generate electricity through a p-i-n junction.

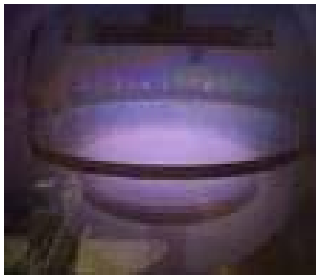


Figure 1.3.4 PEVCD in Process[19]

The p-i-n junction is the mechanism that allows an a-Si solar cell to create electricity. There are three layers to the p-i-n structure. Impurities are applied to a-Si:H in a process called doping, and this can cause the a-Si:H to be more negatively or positively charged. The top layer is a positive (p) doped a-Si, an undoped a-Si layer is the middle layer, called intrinsic (i), and a negatively (n) doped a-Si layer is on the bottom.[20] This sandwich of layers provides the mechanism to create the electrical current. In a p-i-n structure, as seen in Figure 1.3.5, an electric field is set up between the p-layer and the n-layer. This electrical field stretches across the middle i-layer of intrinsic silicon, which is the resistive region.[21] The glass (substrate) layer of the cell allows light to pass through while protecting the wafer. The front contact is made up of grid-like metal contacts. The reflection enhancement layer acts to increase the amount of light absorbed into the solar cell. The back contact provides a full area of metal contact covering the entire rear side of the cell to allow metal electrodes to be in contact with the silicon.[22] Silicon is a relatively poor conducting material when compared to metallic materials, and there would be little electrical current generated if a solar cell depended on diffusion. With the p-i-n structure, however, light generates free electrons and holes, or complementary positive charges that flow in the opposite direction of the electrons, that are injected from the p-layer and n-layer regions into the i-layer. The current flows because the free electrons and holes are being generated within an electrical field, rather than moving toward the field. The amount of current generated depends on both geometry and the nature of the material in the resistive i-layer region of the cell.[21] For instance, the

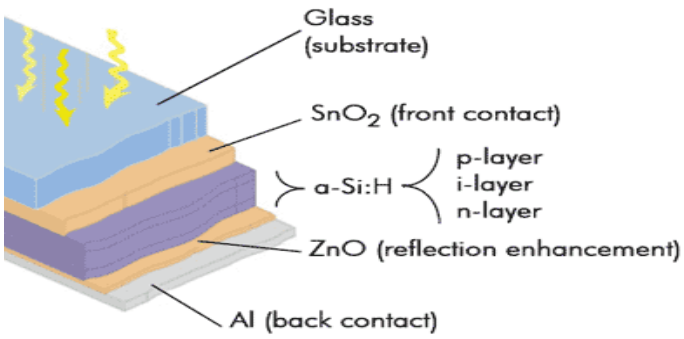


Figure 1.3.5 Cross Section of Thin-Film a-Si:H Solar Cell[23]

energy for the p-i-n junction is greater because amorphous silicon has defects at the atomic level which make it highly conductive at a greater band than crystalline silicon would be.[3] The effectiveness of a solar cell is determined by the energy conversion efficiency[20] (η, "eta"). This represents the amount of absorbed light that is converted to electrical current. The percentage is calculated, as demonstrated in Figure 1.3.6, using the ratio of the maximum power point, Pm in W, divided by the input light irradiance, E in W/m^2, times the solar surface area, Ac in m^2.

$$\eta = \frac{P_m}{E \times A_c}$$

This would be accurate under normal test conditions.[24] Amorphous silicon cells are the least efficient of the solar cell types, but this is offset by the low cost of production, allowing these cells to still be cost effective, as seen in Figure 1.3.7.

Table I. Confirmed terrestrial cell and submodule efficiencies measured under the global AM1.5 spectrum (1000 W/m^2) at 25°C (IEC 60904-3: 2008, ASTM G-173-03 global)

Classification[a]	Effic.[b] (%)	Area[c] (cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF[d] (%)	Test centre[e] (and date)	Description
Silicon							
Si (crystalline)	**25.0 ± 0.5**	4.00 (da)	0.705	**42.7**	82.8	Sandia (3/99)[f]	UNSW PERL[12]
Si (multicrystalline)	**20.4 ± 0.5**	1.002 (ap)	0.664	**38.0**	80.9	NREL (5/04)[f]	FhG-ISE[13]
Si (thin film transfer)	**16.7 ± 0.4**	4.017 (ap)	0.645	**33.0**	78.2	FhG-ISE (7/01)[f]	U. Stuttgart (45 μm thick)[14]
Si (thin film submodule)	**10.5 ± 0.3**	94.0 (ap)	0.492[g]	**29.7**[g]	72.1	FhG-ISE (8/07)[f]	CSG Solar (1-2 μm on glass; 20 cells)[15]
III-V cells							
GaAs (crystalline)	**26.1 ± 0.8**	0.998 (ap)	1.038	**29.7**	84.7	FhG-ISE (12/07)[f]	Radboud U. Nijmegen[6]
GaAs (thin film)	**26.1 ± 0.8**	**1.001 (ap)**	**1.045**	**29.5**	**84.6**	**FhG-ISE (07/08)[f]**	**Radboud U. Nijmegen[6]**
GaAs (multicrystalline)	**18.4 ± 0.5**	4.011 (t)	0.994	**23.2**	79.7	NREL (11/95)[f]	RTI, Ge substrate[16]
InP (crystalline)	**22.1 ± 0.7**	4.02 (t)	0.878	**29.5**	85.4	NREL (4/90)[f]	Spire, epitaxial[17]
Thin film chalcogenide							
CIGS (cell)	**19.4 ± 0.6**[h]	0.994 (ap)	0.716	**33.7**	80.3	NREL (1/08)[f]	NREL, CIGS on glass[18]
CIGS (submodule)	**16.7 ± 0.4**	16.0 (ap)	0.661[g]	**33.6**[g]	75.1	FhG-ISE (3/00)[f]	U. Uppsala, 4 serial cells[19]
[illegible]							
Amorphous/nanocrystalline Si							
Si (amorphous)	9.5 ± 0.3[i]	1.070 (ap)	0.859	17.5	63.0	NREL (4/03)[f]	U. Neuchatel[21]
[illegible]							
Photochemical							
Dye sensitised	10.4 ± 0.3[k]	1.004 (ap)	0.729	**22.0**	65.2	AIST (8/05)[f]	Sharp[23]
Dye sensitised (submodule)	8.2 ± 0.3[k]	25.45 (ap)	**0.705**[g]	**19.1**[g]	61.1	AIST (12/07)[f]	Sharp, 9 serial cells[24]
Dye sensitised (submodule)	8.2 ± 0.3[k]	18.50	0.659[g]	**19.9**[g]	62.9	AIST (6/08)[f]	Sony, 8 serial cells[25]
Organic							
Organic polymer	5.15 ± 0.3[k]	1.021 (ap)	0.876	**9.39**	62.5	NREL (12/06)[f]	Konarka[26]
Organic (submodule)	1.1 ± 0.3[k]	232.8 (ap)	29.3	0.072	51.2	NREL (3/08)[f]	Plextronics (P3HT/PCBM)[27]
Multijunction devices							
GaInP/GaAs/Ge	32.0 ± 1.5[j]	3.989 (t)	2.622	14.37	85.0	NREL (1/03)	Spectrolab (monolithic)
GaInP/GaAs	30.3[j]	4.0 (t)	2.488	14.22	85.6	JQA (4/96)	Japan Energy (monolithic)[28]
GaAs/CIS (thin film)	25.8 ± 1.3[j]	4.00 (t)	—	—	—	NREL (11/89)	Kopin/Boeing (4 terminal)[29]
a-Si/μc-Si (thin submodule)[j,l]	11.7 ± 0.4[j,l]	14.23 (ap)	5.462	2.99	71.3	AIST (9/04)	Kaneka (thin film)[30]

Figure 1.3.6 Solar Efficiency Record[25]

1.4 Previous Research on Amorphous Silicon Solar Cells

Advances have been made in a-Si:H solar cells since the original research by Carlson and Wronski in 1976. Areas of investigation have included materials, device structures, and the manufacturing process of a-Si.[7] New materials have been added to a-Si to increase the efficiency of amorphous solar cells,[7] such as a-Si:C:H using CH_4. Reflective materials have also been added to the back of thin film cells to increase the light input, which helps, in turn, to increase the efficiency of the solar cell. Combining multiple layers of

thin film a-Si solar cells is now possible with multiple p/n junctions using wider spectrums of light to provide higher efficiencies for electrical output. In a photovoltaic cell, the band gap will determine which portion of the solar spectrum will be absorbed by the cell.[26] If the solar cell is constructed with layered materials, the band gap can be altered to achieve greater conductivity. If the gap between the valence and the conductive bands is small enough, electrons that gain energy by absorbing light can jump from one band to another. Having even a small amount of doping material present will significantly increase this conductivity.[27] The manufacturing process for a-Si:H solar cells has been refined to determine the optimum layer thickness for the p-i-n layers, as well as to reduce the Staebler-Wronski Effect.[17] These advances in the creation of new methods for manufacturing a-Si solar cells have required years of research and significant cost.

1.5 Previous Research on Vertical Structures

Additional research other than that related to solar cells has been completed in relation to vertical silicon structures. A particular portion of this vertical structure research involves antireflection coatings (ARC).[28] None of the existing research has integrated the vertical structures into the p-i-n junction. Vertical structures have been used as an ARC because a major problem with crystalline silicon solar cells is the shiny nature of crystalline silicon, as it is much like polished glass. This results in reflection of light off of the surface of the cell. Up to 30% of the light can be reflected back, and this unabsorbed light results in a loss of potential energy. [28] One way to reduce the reflection from the solar cell is to include an antireflective layer with an uneven surface. An example of a natural occurrence of this method for antireflection is seen in the structure of the eye of a moth.

This insect's eye has multiple bumps on the cornea, known as nipples, which are arrayed in a hexagonal shape. (Figure 1.5.1) This reduces the reflection and allows a moth's eye to efficiently capture light.[28] There have been multiple attempts to duplicate this uneven surface by using a model of the structure of a moth's eye to act as an ARC. The experimental processes have resulted in a reflection rate of less than two percent. The first attempts to use the moth's eye structure to create the requisite uneven surface have met with some success. However, it is an expensive process when using crystalline silicon.[28] Additionally, research has been done in which polymer dots in a colloidal crystal polymer nanocomposite were spun on silicon and then a series of steps was employed to etch back the dots and create a moth-eye structure. This method is a less expensive way of producing a moth-eye structure silicon pillar array.[29] (Figure 1.5.2) Despite these advances, there is currently no commercial manufacturing method for vertical moth-eye structures.

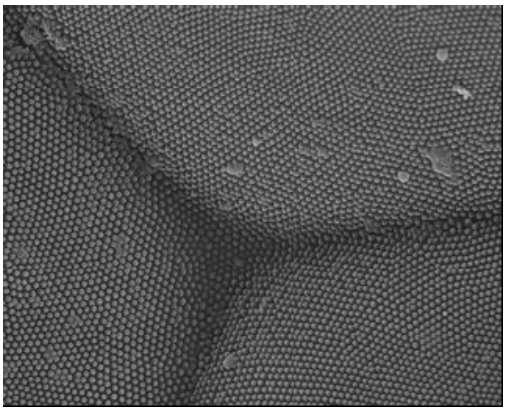


Figure 1.5.1 Moth Eye Structure[30]

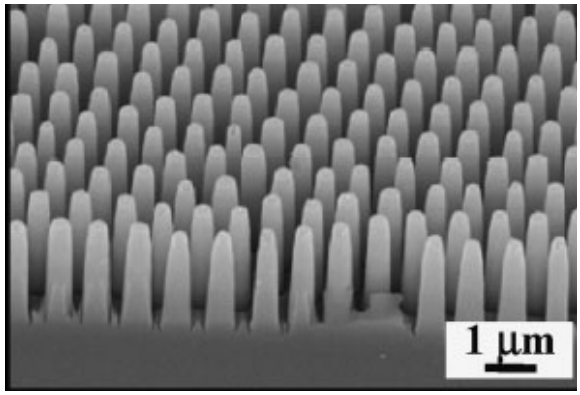


Figure 1.5.2 Silicon Pillar Array[28]

1.6 Research Goals

It is theorized that vertical structures could not only be used in the ARC of the solar cell, but could also increase the efficiency when incorporated into other components of the cell. Traditional a-Si thin film solar cells employ a planar structure to absorb incident light. It is proposed that the planar structures be replaced with vertical 3-D structures. In addition to the antireflection benefits, the vertical structure model increases the efficiency of light absorption by lengthening the optical absorption path and reducing electron trapping. The purpose of this capstone project is to employ photolithography to create a vertical structure mold that incorporates this methodology through an inexpensive process. Figure 1.6.1 illustrates the advantage of the proposed structure when compared with traditional planar construction.

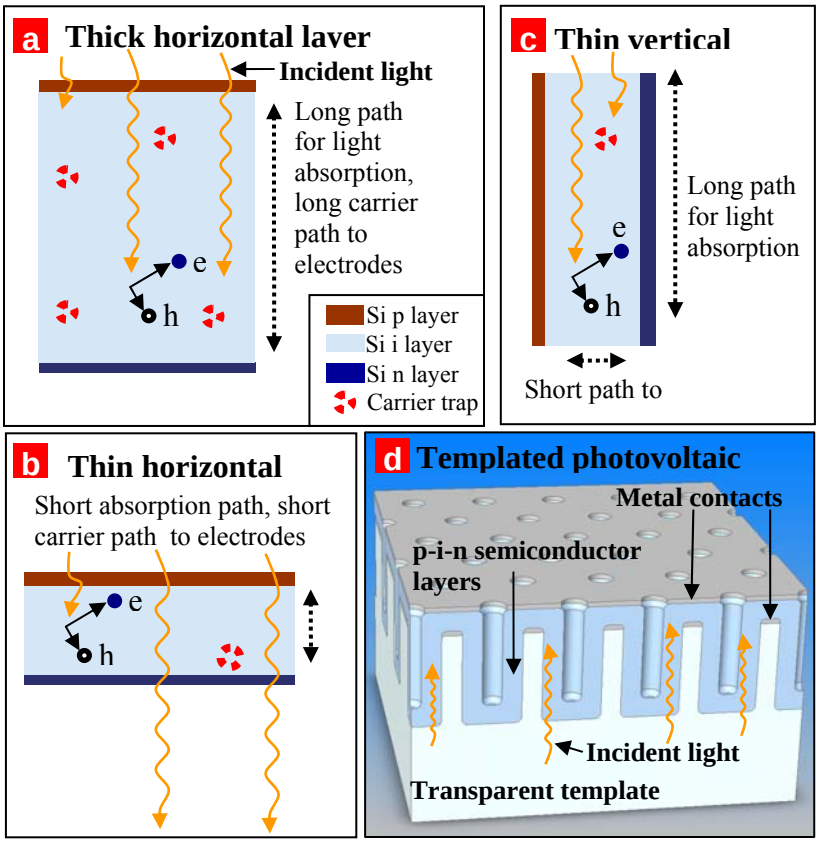


Figure 1.6.1 Planar vs. 3D photovoltaic layers Blue and red layers represent highly doped p and n layers that the electrons and holes (charge carriers) must reach before recombining. Traps in the intrinsic i layer reduce carrier mobility and increase recombination. **a,** Thick horizontal layers have more complete light absorption. However, carriers must travel through this thick absorption layer resulting in recombination losses. **b,** Thinner horizontal layers reduce the distance carriers must successfully travel but suffer from incomplete absorption. **c,** The thin-layer vertical geometry provides a short path for carrier extraction, high extraction field, and corresponding short carrier separation time, thus reducing carrier loss from recombination while maintaining a long absorption path. **d**, Vertical layers can cost effectively fabricated by conformal plasma enhanced chemical vapor deposition (PECVD) on templates. Deposited device layers take on the three dimensional shape of the nanostructured transparent template. [31]

This project focuses on the elements labeled (c) and (d) in Figure 1.6.1. The mold is modeled after a moth-eye structure to create narrow pillars and reduce reflection, thus bringing more light into the solar cell. In addition, the longer, narrow structure would increase the path length, resulting in more light absorption. A mold on the order of 1 to 3 microns thick would be used to create solar cells on glass with applied a-Si:H doped to create the p-i-n junction to generate electricity. Most thin film a-Si:H solar cells are on

the order of 100 nanometers thick, so any attempt to work with 1to 3 microns is stretching the boundaries. The mold was planned to be made of glass with aluminum contacts, which would provide additional reflection and increase the light focused on the cell. In theory, the cell would be less costly to create because of using a-Si on glass. This is less expensive compared to c-Si and poly-Si because the cost of materials is less and a smaller amount of materials is required. The planned process for achieving the goal of a reusable mold ran into difficulties which resulted in a need to reevaluate and, ultimately, the planning of a new process under the direction of the faculty advisors.

Chapter 2

2 Materials and Methods

2.1 Processing of HSQ Design

The original process centered on spinning on a 3 micron layer of negative photoresist SU-8 10, a viscous polymer, onto a silicon wafer. The photoresist would be baked, and then exposed to UV light using two photomasks, one in the ratio of one to five (1:5) and one in the ratio of two and one-half to three and one-half microns (2.5:3.5). After exposure, the photoresist would be developed. Hydrogen silsesquioxane (HSQ), an inorganic polymer and electron beam resist, would be applied in a spinning process in order to fill the trenches and leave a thin coating on the peaks. Samples would be characterized using an atomic force microscope (AFM) to differentiate the height between a rib and a filled trough, which would, in turn, indicate how much HSQ to etch back.

The thin top layer of HSQ would be etched back to expose the tops of the peaks of photoresist using tetramethylammonium hydroxide (TMAH). This would leave the wafer with the photoresist pattern and the HSQ filling in any of the spaces left by the pattern. The HSQ would be baked to convert it to silicon dioxide, hardening the mold. The final step would be to remove the photoresist with O_2 plasma, called ashing, and this would leave a pattern of lines and trenches in silicon dioxide on top of a silicon wafer, as seen in

Figure 2.1.1. The silicon wafer could be replaced with a glass wafer after initial testing. This would produce a reusable glass mold.

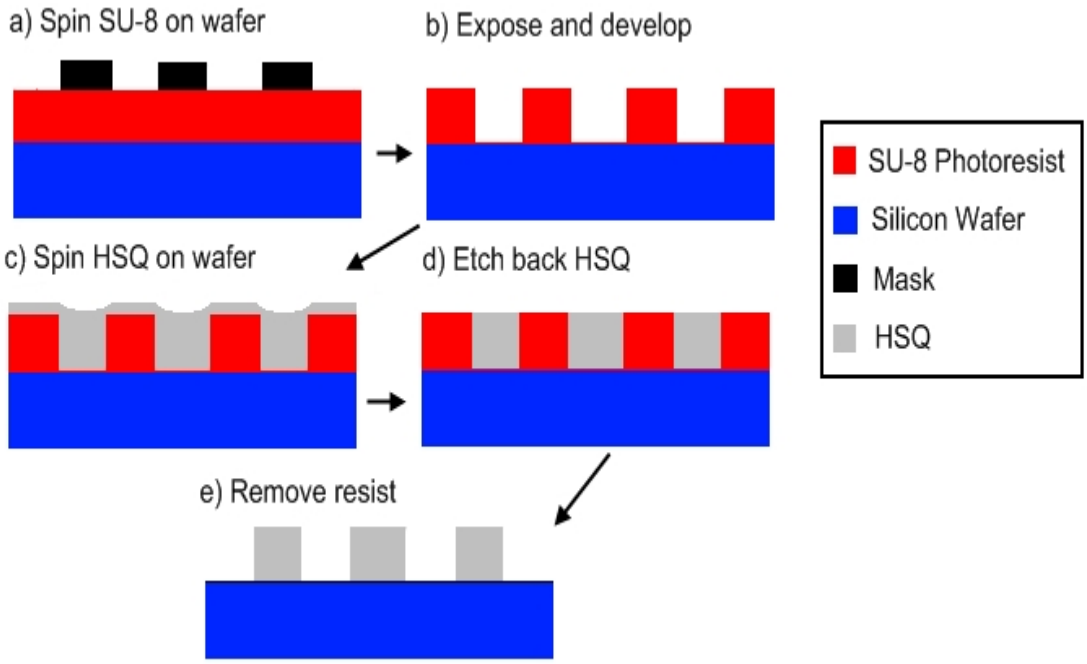


Figure 2.1.1 HSQ Mold Design

2.2 Detail of Initial Procedure with HSQ

1. Prepare wafer for photoresist
   - Clean with acetone and isopropyl alcohol (IPA) on a spinner
   - Bake at 200°C on hotplate for 5 minutes or in oven for 120°C for 10 minutes

2. Apply photoresist as displayed in Figure 2.1.1 a
   - Apply hexamethyldisilazane (HMDS) as an adhesion promoter
     - Mount 4" silicon wafer on Laurell spinner
     - Apply 4 drops HMDS adhesion promoter
     - Spin at 3000 rpm for 10 seconds
   - Apply quarter sized amount of SU-8 10 negative photoresist
     - (approximately 1 ml. per inch of substrate diameter)
     - Spin at 4250 rpm for 2 minutes

3. Soft bake
   - Bake wafer on hotplate for 5 minutes at 65°C
   - Bake an additional 5 minutes at 95°C

4. Expose to UV light using mask aligner 17 seconds hard contact as displayed in Figure 2.1.1 b
   (place mask with lined pattern of 1:5 or 2.5:3.5 microns on top)

5. Post expose bake
   1 minute at 65°C and then 2 minutes at 95°C

6. Develop with SU-8 developer
   Place in developer bath for 45 seconds
   Quickly remove, rinse the wafer with IPA
   Blow dry with N_2

7. May be hard baked
   150°C to 200°C

8. Prepare wafer for HSQ
   Bake at 200°C for 1 minute

9. Apply HSQ as displayed in Figure 2.1.1 c
   Spin at 1200 rpm for 30 seconds

10. Bake at 120°C for 10 minutes

11. View lithography sample
   Cut off piece of 4" wafer
   View lithography test piece with microscope

12. Etch back HSQ as displayed in Figure 2.1.1 d
   Etch HSQ with 20% tetramethylammonium hydroxide (TMAH) solution
   Etches at 18.9 nanometers/second when TMAH solution is at 95°C to 100°C
   Review sample in optical microscope

Though steps 13 and 14 were part of the initial planned process, they were not completed because of the poor results achieved in steps 11 and 12. These final two steps are included only as reference.

13. Remove SU-8 10 photoresist as displayed in Figure 2.1.1 e
   Use complete ashing or piranha etch or plasma etch process

14. Heat treatment to convert HSQ to silicon dioxide
   Bake at 300°C for extended time

2.3 Preliminary Processing of Polyimide Design

After problems developed while working with the HSQ mold design during the summer and fall of 2008, the original experimental design was reevaluated and a second experimental process was proposed in early 2009. The goal was still to make a reusable mold, but with the use of different processes and materials. The newly proposed process centers on making a reusable mold out of polyimide, a strong and heat resistant polymer, with lines and spaces on the micron scale. It was necessary to procure from HD MicroSystems a usable form of polyimide, since this was not readily available at BYU. Obtaining polyimide in an inexpensive quantity was challenging, and ensuring the polymer was appropriately transported and stored (at a low enough temperature to guarantee its efficacy) was essential. Once available, polyimide would be spun onto silicon wafers and cured. Photoresist AZ 3300, a positive photoresist, was planned to be spun on top of the polyimide and baked, then exposed with UV light using photolithography with a photomask with one and one-half micron scale boxes and lines. This would require a new photomask not available at BYU, and at a much smaller level than used in the HSQ design the previous year.

Designing the photomask required obtaining freeware integrated circuit layout design software, and learning how to use this computer application. Once the model was created, it was necessary to find a photomask designer who would collaborate in transferring the design into a workable photomask. The next step would be to cover the photoresist pattern and polyimide with aluminum applied by evaporation. An ellipsometer would be used to measure the thickness. The remaining photoresist would then be removed leaving aluminum patterns on top of polyimide. The polyimide that is not covered by aluminum

would be etched off with oxygen plasma. In theory, this would leave a three micron pattern on top of the silicon wafer in polyimide coated in aluminum. (Figure 2.3.1) Silicon wafers could be replaced by transparent glass wafers.

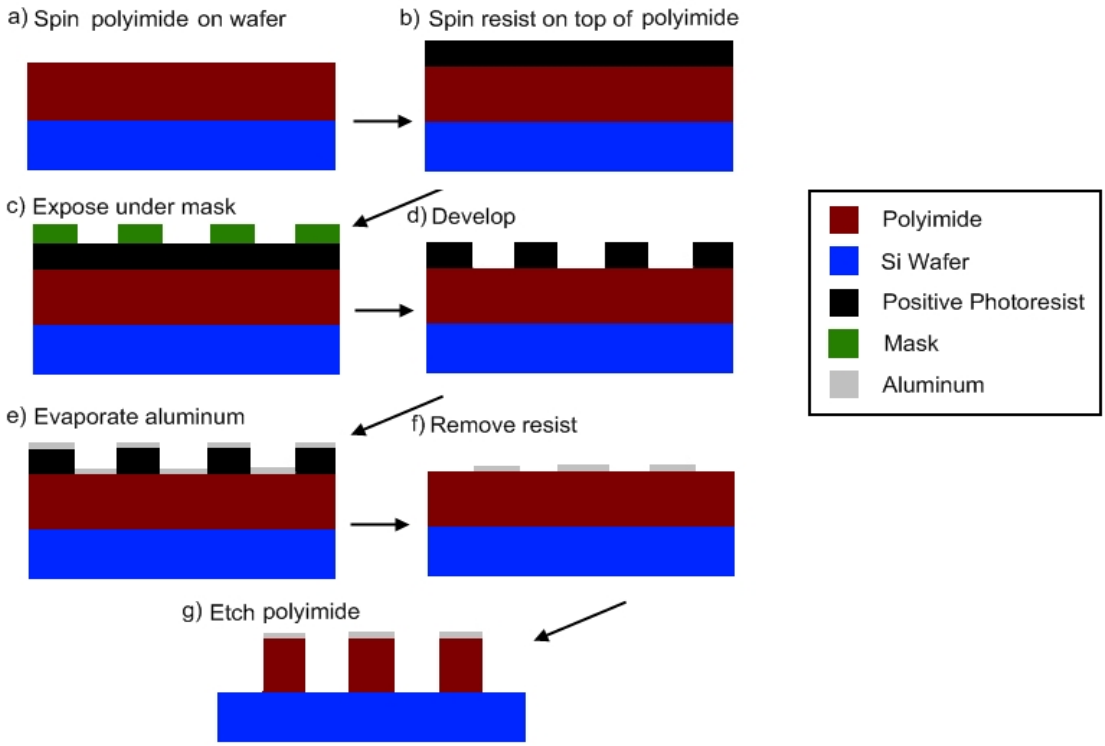


Figure 2.3.1 Polyimide Mold Design

2.4 Detail of Proposed Procedure with Polyimide

1. Prepare wafer for polyimide
   Clean with acetone and isopropyl alcohol (IPA)
   Bake at 120°C for 10 minutes

2. Apply polyimide as displayed in Figure 2.3.1 a
   Place silicon wafer piece on spinner
   Apply quarter sized amount of polyimide
   Spin at 3000 rpm for 60 seconds

3. Bake
   Bake on hotplate at 90°C for 30 minutes

4. Measure thickness of polyimide
   Measure using ellipsometer and/or AFM

5. Apply photoresist as displayed in Figure 2.3.1 b
   Apply an adhesion promoter HNDS
   Spin at 3000 rpm for 10 seconds
   Apply positive photoresist AZ3312
   Spin at 3000 rpm for a thickness of 1250 nanometers

6. Soft bake
   90°C for 60 seconds

7. Expose to UV light using 1:5 mask as displayed in Figure 2.3.1 c
   Expose 4 to 5 seconds

8. Develop exposed photoresist on wafer using AZ300MIF as displayed in Figure 2.3.1 d
   Develop for 30 to 40 seconds

9. Post exposure bake
   Bake at 90°C for 60 seconds

10. View lithography sample
   View lithography test piece in optical microscope

11. Evaporate aluminum as displayed in Figure 2.3.1 e
   Evaporate aluminum on wafer using thermal evaporator

12. Lift off AZ3312 photoresist as displayed in Figure 2.3.1 f
   Remove photoresist with solvent etch

13. Remove excess polyimide as displayed in Figure 2.3.1 g
   Remove excess polyimide with oxygen plasma etch with PE2 plasma etcher

14. View lithography sample
   View lithography test piece in optical microscope

2.5 Designing Photomask

An integral part of preparing for the proposed procedure with polyimide was designing the photomask. A computer-aided design (CAD) software application was needed. The first to be investigated was LayoutEditor. The default size with this program is 1 micron =1 unit. For the proposed process, a 4 inch by 4 inch mask pattern with a different pattern in each one inch quadrant was required. As the attempted construction

of the photomask continued, LayoutEditor did not seem to have the required functionality.

Since this project would not support the purchase of software applications, a freeware CAD editor was the only option. One application, Electric, was found to be more user friendly than LayoutEditor. Electric contains a tool much like Microsoft's "Paint." However, it did not have a grid system. Transferring the file to a GDSII format revealed that the boxes on the model did not line up to the grid pattern the photomask required. This necessitated a return to LayoutEditor. Unfortunately, to make even a 1 inch by 1 inch quadrant, one-fourth the size of the photomask specifications, requires a 25,400 by 25,400 micron square. The memory capacity of the available desktop computer was not sufficient to sustain the process. Even allowing LayoutEditor unlimited memory allocation would not support creating the pattern.

The next trial was to use the cell feature of the GDSII file format. In a new cell a command can be used to paste a reference from another cell at the new location. The hope was that the memory would be able to sustain the paste feature, but this was not the case. The required memory capacity was equal to simply creating the entire pattern. The cell feature did allow for each change to be referenced to all other cells automatically, but the memory requirement remained unchanged. Features of Electric were tried once more with a new approach, but it was also unsuccessful. The next trial was again with LayoutEditor. A small version of the pattern for all four quadrants was attempted, with 1 micron boxes (in a 1000 square micron area). Next, .5 (one-half) micron boxes next to the smaller version were created.

The final step, however, required lines to be crisscrossed in a hexagonal pattern. The angles were determined using a computer drawing tool, and the lines needed to be slanted at either 60 or 120 degrees, depending upon which side was used as the measuring point. This proved to be a problem in LayoutEditor, since once the program slanted a line it turned the box into a polygon and it was then impossible to adjust either length or width. As a result, the lines extended outside the pattern box with no way to delete the extensions. There is no "crop" feature in the program. The next step was to use 1 micron lines in one quadrant and another quadrant with .5 (one-half) micron lines. The result was not neat, but the basic idea was clearly evident.

Each of the quadrants had been done in a different cell, so the last step was to construct a final cell and reference each of the quadrants in order to achieve the entire pattern. Screenshots were used to inspect the finished pattern (Figures 2.5.1-2.5.3).

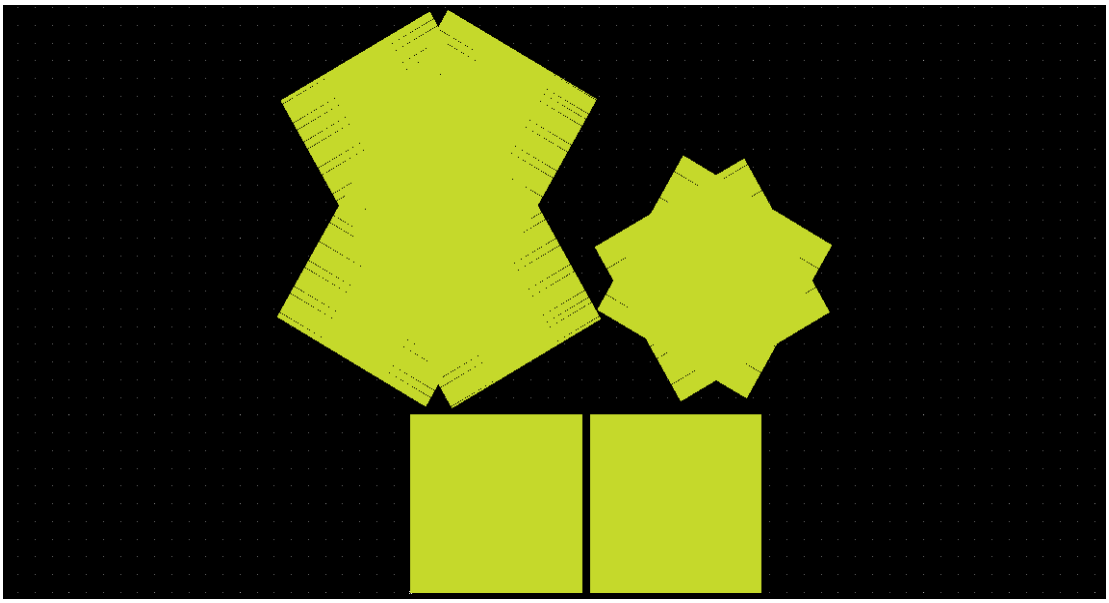
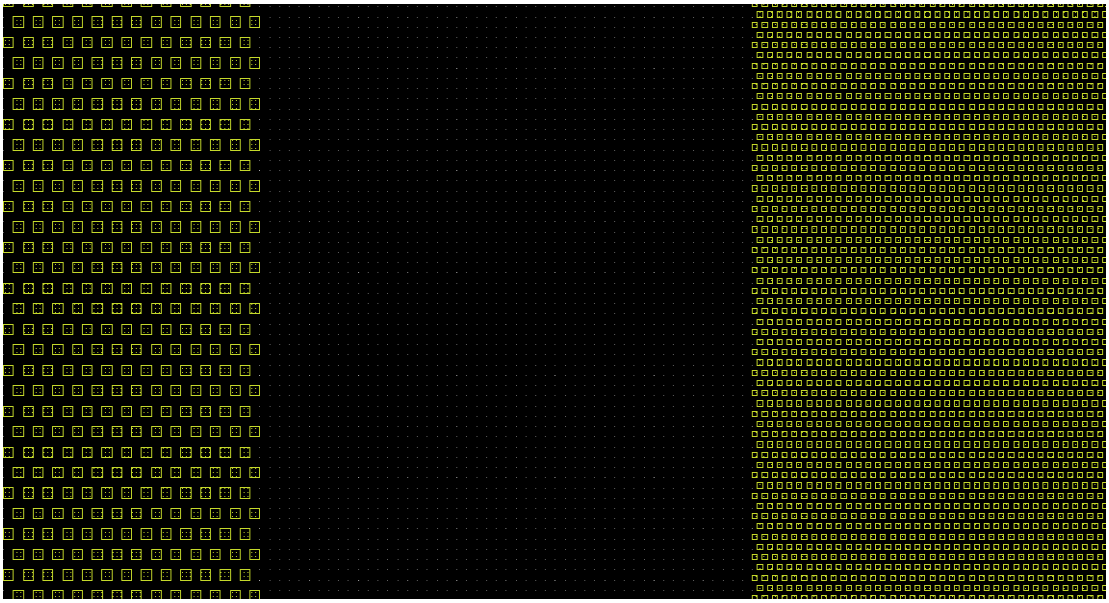


Figure 2.5.1 (Above) At a distance, the grid pattern in the final design, cannot be distinguished.

Figure 2.5.2 (Below) A close-up of the 1 and the .5 quadrant boxes.



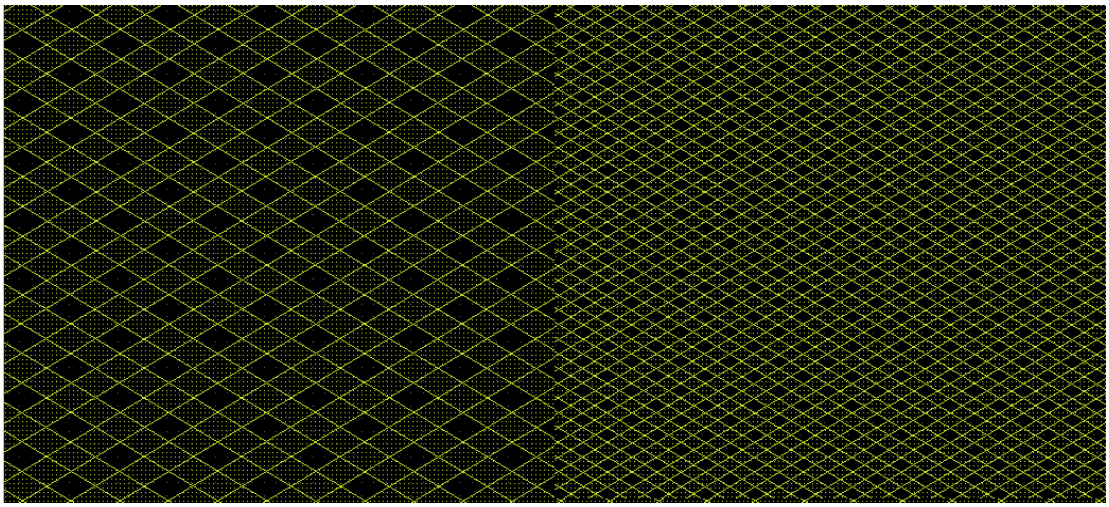


Figure 2.5.3 A close-up of the grid pattern lines in the 1 and the .5 micron boxes.

The result was saved as a GDSII file with a size over 80 megabytes. The commercial photomask company that was contacted for a price quote first suggested sending the file in a DXF format. Research revealed that DXF is another format for CAD files. After converting the GDSII file to a DXF file, the required memory was one-half of a gigabyte, far too large to send to the company. Returning to the GDSII format and zipping the file before sending seemed a more effective solution. This resulted in a file size of 15 megabytes, which was still too large. The file had to be adjusted, deleting some of the boxes and lines, in order to finally reduce the zipped file size to 5 megabytes. The price quoted by this company proved to be far outside the budget for this project.

Further consultations with the photomask company led to the BYU Department of Electrical and Computer Engineering. Experts recommended using a step and repeat process. This required the creation of a 10 times increased sized mask (half micron becomes 5 microns). Figures 2.5.4 and 2.5.5 are examples of this enlarged pattern.

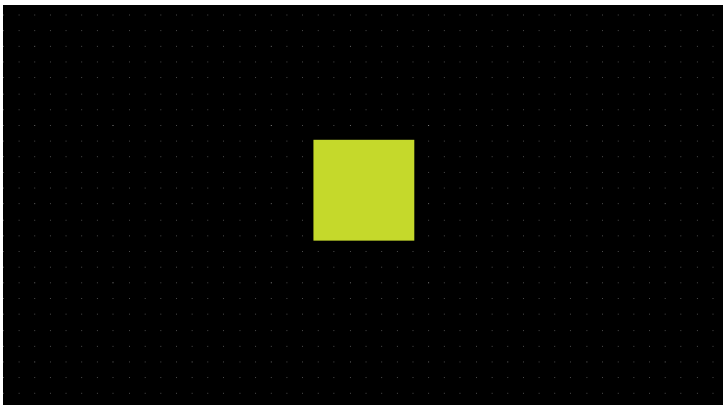


Figure 2.5.4 Quarter inch square (500 grid)

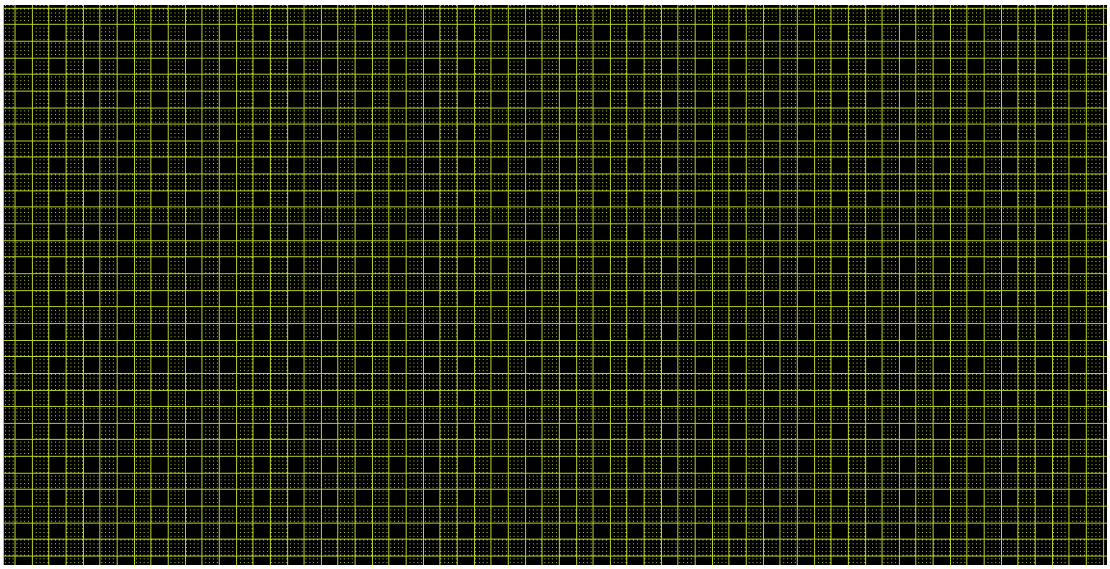


Figure 2.5.5 Close-up of .75 inch design

The step and repeat process reduces this pattern by 10 times onto the substrate which allows for a smaller pattern that is detailed and accurate. This offered a practical and reasonably priced solution which would create a photomask appropriate for the needs of this project. As of the date of this paper, the photomask is in development.

Chapter 3

3 Results and Conclusions

3.1 HSQ Mold Results

Two lithography samples were created using the HSQ mold process. One lithography sample was made using a lined pattern of 1:5 microns and a second was made with a lined pattern of 2.5:3.5 microns. The samples were viewed with the AFM after the initial HSQ was applied after the SU-8 10 was developed. The 1:5 lithography sample did not have a consistent difference between the level of HSQ in the filled trenches and over the ribs. Looking at several spots, the difference between the top of the trench and the top of the ribs ranged from 203 to 470 nanometers. The 2.5:3.5 lithography sample varied from looking completely planar with no discernable ribs to having blotches where the ribs showed. The blotches could be seen with an optical microscope. In these spots the difference in height between trench and rib was fairly consistent at 40 nanometers. There was also a 40 nanometer height difference between where the trenches showed and the raised planar sections. A scratch was created with a pair of tweezers to reference the total thickness of SU8 and HSQ on the wafer. Viewing the sample through an optical microscope revealed that the total thickness was near 3 microns. At this point, the 1:5 sample was rejected because of the uneven distribution, but the 2.5:3.5 wafer was prepared for the next step in the process. This piece of wafer was etched with TMAH. The TMAH was heated to 95°C. The sample was immersed in the TMAH for 70 seconds because of the thickness of the HSQ, and then rinsed with IPA. Discoloration was

evident after the rinsing. Review under an optical microscope revealed indistinct lines with little definition. It appeared that the lithography patterns were unusable and the HSQ process was stopped until further consultation with the faculty advisors on using a different process and materials.

3.2 Creating Photomask Results

The creation of the photomask pattern was achieved using CAD freeware. The company, IC Photomask, was extremely helpful in providing a contact with the BYU Electrical and Computer Engineering Department. While it may take several weeks to complete the photomask, it will be done to specifications and within the project's budget. Because the photomask is not yet ready for use, only the first four steps of the polyimide process have been completed.

3.3 Polyimide Results

Polyimide for optical uses must be refrigerated at -18°C (freezer temperature) and has a shelf life of one or more years, but it is only stable for 2 weeks at room temperature. In the coming weeks, three tests are planned to observe the properties of polyimide. First, the polyimide will be used to determine optimum spin speeds and baking temperatures for 300 nanometer thicknesses. If a thinner layer of polyimide is used, the ellipsometer can be used for measurement. The next question that needs to be addressed is how sensitive polyimide is to the photoresist developer that will be used. This must be determined for both soft and hard baking. Finally, the speed at which the O_2 plasma etches the polyimide must be determined for both the soft and hard bake stages. Polyimide was received from HD MicroSystems in order to continue with the research.

Polyimide was spun on silicon wafers at 8000 RPM for 30 seconds. Five samples were spun at this speed and soft baked at 100°C on a hotplate for varying lengths of time. The heights were measured using an AFM and the results are reported in Figure 3.3.1.

Length of Soft Bake	Height
30 minutes	1463 nm
45 minutes (sample 1)	1278 nm
45 minutes (sample 2)	1058 nm
60 minutes (sample 1)	1535 nm
60 minutes (sample 2)	1379 nm

Figure 3.3.1 Comparison of Height and Soft Bake Time

3.4 Conclusions

The goal of creating a less costly process of patterning vertical structures in a-Si is still a work in progress, but now shows real promise. When I began working on the process one year ago, the expectation was that usable research results would be obtained within a few weeks. However, the first weeks of work I completed on the HSQ mold design showed process flaws. The problem was with the lithography of photoresist SU-8 10 at 3 micron layers. The lithography pattern viewable only by an electron microscope showed an unusable pattern with unclean lines and definition. As a result, I consulted with my faculty advisors and we decided the process should be stopped after applying the HSQ because the pattern was flawed. The 3 micron layer photoresist thickness required using an electron microscope to discover the pattern problems, a very time consuming

procedure for me. This initial portion of the research was an important part of advancing the project as a whole, but did not provide me with any usable research results that could be reported. After a discussion of these issues with my advisors, I worked on a second process and plan for creating a mold using different materials and processing.

After doing some research, I was able to locate and bring to BYU a supply of polyimide. Polyimide was first used as nylon 66 in the 1930s and has since been used as a heat insulator for electronics. It provides the material that is used for making Kevlar for bullet proof vests.[32] In the second process I used polyimide as a base to apply a much thinner layer of photoresist, no more than 1 micron. This allowed the pattern to be reviewed by an optical microscope, which provided a much faster review process than when an electron microscope was used. Also, with a thinner photoresist layer there was a higher probability that the pattern would develop all the way through the photoresist and provide a clean pattern that could be repeated. In addition, polyimide is a very durable polymer and is used in situations where durability and resistance to heat is necessary and it should provide a good base to the vertical pattern. This proved to be a good choice, as seen in the results obtained when I spun the polyimide, used the soft bake, and completed measurements with the AFM. I also discovered that contact lithography might be a more effective process for this research. The photomask which I designed and created the pattern for has not been completed. Creation of the photomask has taken several weeks longer than the original estimated completion date. This meant the use of the polyimide mold had to be assigned to someone else. I provided training for this student over a period of four weeks in order to smoothly transition the last stages of the research.

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