SELECTIVELY GROWN SILICON NANOWIRES FOR TRANSISTOR DEVICES

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ABSTRACT

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The goal of this project is to enable fabrication of a transistor device using silicon nanowires (SiNW) as semiconductors. In order to be able to establish electrical contact with the nanowires the SiNW growth is confined to certain areas that can be contacted using electron-beam lithography (EBL). This is done by controlling the deposition of SiNW catalyst through angle-evaporation onto pillars on the device. The nanowires then grow from the sidewalls of the pillars and can be contacted using EBL.

ACKNOWLEDGMENTS

Contents

List of Figures

Chapter 1

Introduction

There are many applications for a chemical sensor within NASA's various missions. As we continue to explore our stellar neighbors, knowledge of lunar and planetary chemical content will become increasingly important. NASA has already sent probes to both the Moon and Mars with some limited ability to detect chemicals; however, more advanced chemical detection is a high priority for future missions. If such analysis can be performed using smaller components and lower power consumption then there will be more room for other instruments, equipment and fuel on board future missions.

This project helps develop a transistor concentration analyzer that is part of an idea known as "lab-on-a-chip" (LOC) in which a number of nano- and microscaled sensors are fabricated on a single chip to provide several forms of chemical analysis from one device. The chemical sensor LOC design includes a liquid chromatography column, a transistor concentration analyzer, and a time of flight mass spectrometer. Such a device would use less power and take up less space on a spacecraft than traditional chemical sensors.

A basic field effect transistor (FET) consists of a semiconductor with electrical
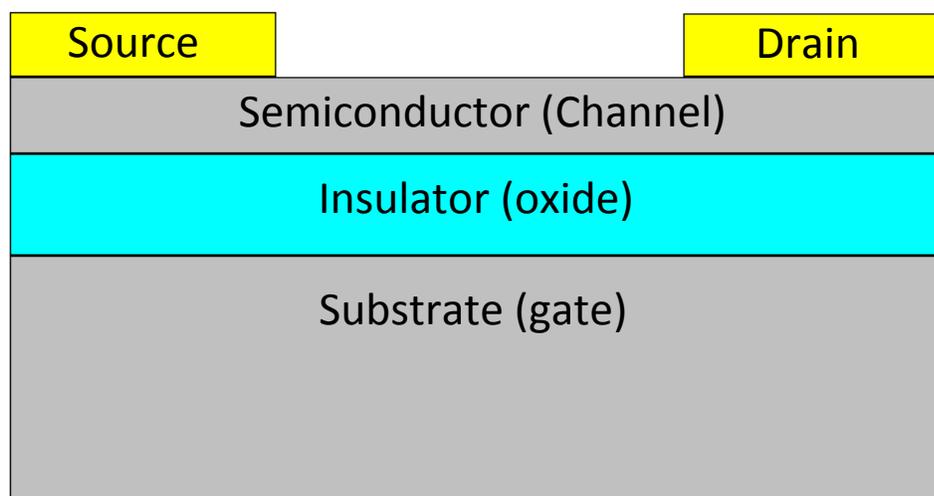
Figure 1.1 A model of a field effect transistor (FET). The semiconductor channel will only allow current to pass from the source to the drain when there is an additional voltage applied to the gate. This gate voltage forces the charge carriers to congregate on one side of the channel: when there are enough carriers present current can begin to flow.

contacts (source and drain) at either end so that a potential can be applied across it (see figure 1.1). At low potential difference there are not quite enough charge carriers (electrons or holes) in the semiconductor to carry a steady current between the leads of the device. When a voltage is applied from the top to the bottom of the transistor the available charge carriers tend to clump at the top or bottom of the semiconductor (depending on the sign of the charges and the direction of the field), forming a conductive "channel." When this second voltage (called a gate voltage) is strong enough, current can flow between the source and the drain. The higher the gate voltage, the greater the accumulation of charge carriers in the channel and the higher the current through the device. [1] Additionally the semiconductor can be doped (adding atoms which contribute additional charge carriers) to increase the conductivity of the device under the influence of a gate voltage.

Silicon nanowires (SiNW) are a viable option for the semiconductor channel in

a transistor device [2] for a chemical concentration analyzer on a lab-on-a-chip sensor(see figures 1.1, 1.2). Silicon nanowires are cylindrical, crystalline silicon structures with diameters on the order of nanometers and lengths up to millimeters. They retain many of the properties of bulk silicon, most notably semiconductivity. [3, 4] They can be produced in a number of ways including suspension, chemical vapor deposition (CVD) and vapor liquid solid (VLS) synthesis. Because of their large length to width ratio, they are the subject of many investigations for use in nanoscale semiconductor devices. [5] To use silicon nanowires as transistors for the concentration analyzer, the nanowires have to be placed in the exact location on the chip where they will be used. In our group, previous work on SiNW transistors has used nanowires that were grown, extracted, and redeposited on a substrate. But this method requires that each individual nanowire be laboriously imaged, recorded, and contacted. The contacting requires that a unique e-beam lithography (EBL) program be written to contact each wire. Establishing a method of fabricating SiNWs *in situ*—already in the location in which they will be used—is the purpose of this research.

Once SiNW transistors are fabricated as part of the LOC, they will be used as a concentration analyzer. The chemical in question will be mixed into an ionic fluid which is flowed across the transistor channel. Rather than using the substrate to establish the gate voltage for these transistors, the ionized fluid provides the gate voltage [6]. The greater the concentration of the test chemical, the lower the concentration of ions in the fluid, producing a lower gate voltage. This variable gate voltage can be calibrated to measure the concentration of the test chemical in the fluid. When combined with a liquid chromatography column (which separates the recovered sample by chemical species) and a miniaturized mass spectrometer, the LOC will be a useful tool for chemical analysis in future NASA exploration missions.

The goal of this project is to create test structures that will enable the transistors
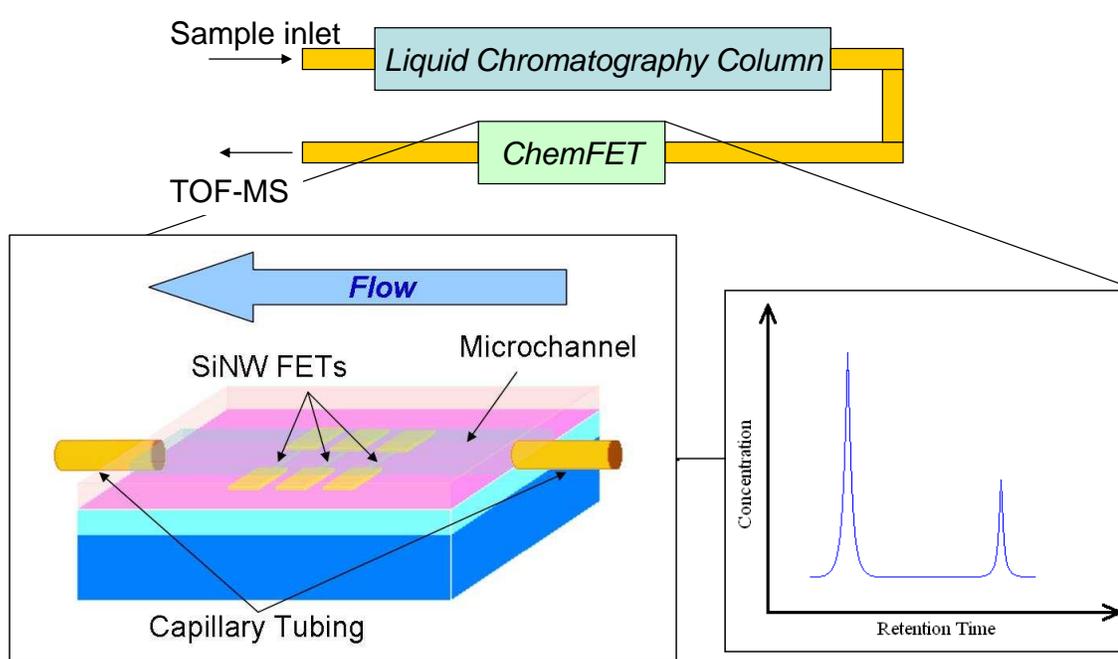
Figure 1.2 Conceptual drawing of a lab on a chip chemical sensor using Si nanowire chemFETs. At the top is a flow chart showing the various devices. As the ionized fluid containing the chemical in question flows over the SiNW FETs, the change in ion density will provide a variable gate voltage, as shown schematically in the graph on the right.

for this LOC device. This will be done by selectively growing silicon nanowires in a desired location on a substrate. These wires can then be doped (or grown pre-doped) with additional charge carriers and used as the semiconducting channel for a transistor device.

Chapter 2

Methods

2.1   Pillar Fabrication

The direct evaporation of gold catalyst onto a substrate produces SiNW growth that is dense across the entire surface of the substrate (see figure 2.1). For the LOC transistors however, it is desirable to limit the SiNW growth to a single nanowire in specific desired locations. To accomplish this we developed a method of controlling the catalyst using microfabrication techniques. The process involves creating small gold squares on a substrate coated with thick thermal oxide, which will then be used to mask an etching process which will leave pillars under the squares. Then we do another gold evaporation onto the sides of the pillars to be used as a catalyst for nanowire growth. The details of these steps follow (see figure 2.2.)

First, the silicon substrate is coated with a thick layer of silicon dioxide (about 4000Å) using wet thermal oxidation at $800\,°C$. Electron beam lithography (EBL) is then used to define small squares (1 μm on a side) in a grid pattern on the substrate. EBL is a lithography process in which electrons—rather than light—are used to define features on a device. It has the advantage that it doesn't use a photo mask and
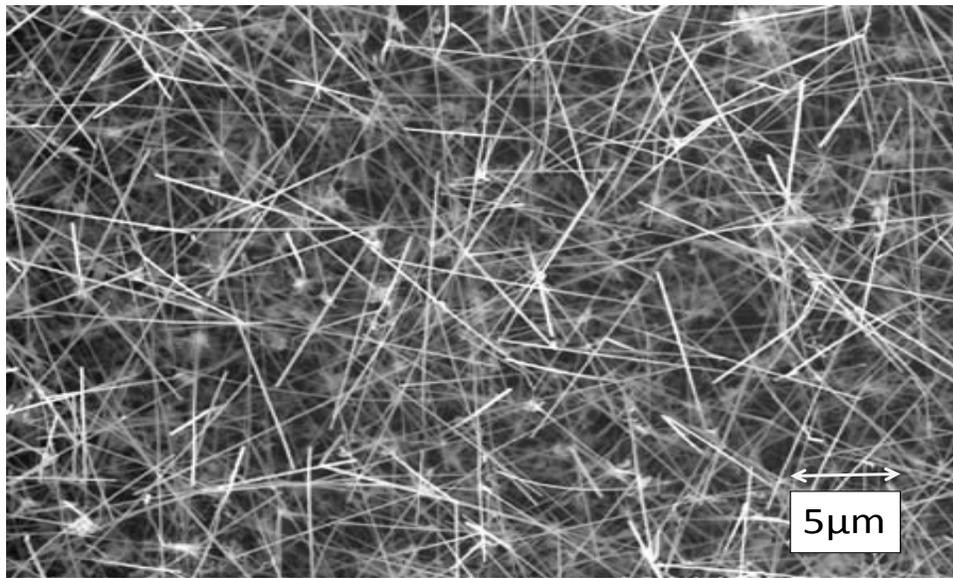
Figure 2.1 A scanning electron microscope image of silicon nanowires grown *en mass* on a silicon dioxide substrate. This method, which uses a thin-film gold catalyst, is relatively easy to re-create; however, it is almost impossible to isolate individual nanowires for devices. Previous methods for isolating nanowires included lifting all of the wires from a substrate like this, suspending them in solution, depositing them on a new substrate, then finding usable wires and building a lithography program to contact them. This pillar process is designed so that single tubes will grow in desired locations.
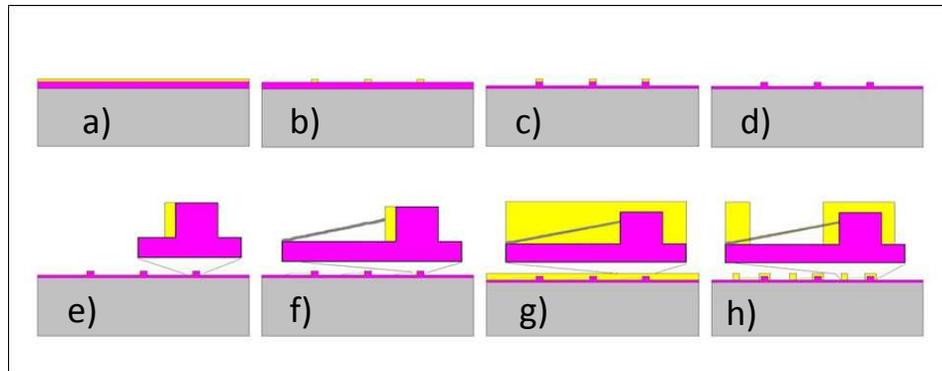
Figure 2.2 A flowchart of the fabrication process. (a) We start with a silicon/silicon dioxide substrate and cover the entire surface with evaporated thin-film gold. (b) Using E-beam lithography we expose and develop the resist leaving small squares of gold (1 μm on a side). (c) Then a reactive ion etcher etches the oxide down about 2400 Å wherever there is no gold etch-stop. (d) The gold is then removed from the tops of the pillars. (e-f) Next we evaporate another layer of gold onto the *sides* of the pillars to be used as catalyst for nanowire growth. (g-h) Once the nanowire has been grown, another lithography/gold evaporation defines contact pads to serve as the source and drain for a transistor device.

therefore can have easily changed patterns (compared to traditional photolithography masks). A pattern—written on design CAD—is then used to control the beam of electrons on a scanning electron microscope to define the pattern. [7] The electrons expose a double-layered (methyl methacrylate/poly-methyl methacrylate) resist. This exposure weakens the polymers in the resist so that when the substrate is immersed in development chemicals the weakened resist desolves leaving the exposed areas open and non–exposed areas protected.

The next step is to create pillars from the exposed squares. Once the pattern of small squares has been developed (leaving the squares open and the rest of the substrate covered), the sample is put into a thermal evaporation chamber. We coat the sample with gold to a thickness of 1000Å. The sample is then removed from the chamber and immersed in an acetone bath to remove the remaining resist. Since the entire sample is coated with gold, there is a thin layer over both the resist and the exposed squares, so when the resist is removed the gold on top of the resist is lifted off as well. This leaves the sample with a grid of small gold squares.

Gold is useful because it is an excellent etch stop for a reactive ion etcher (RIE). RIEs work by taking a gas that is reactive with the sample (such as CF_4), turning it into a plasma and accelerating the ions into the substrate. This provides a very even, unidirectional etch. Since the fluorine ions etch silicon dioxide much faster than they etch gold, the 1000Å gold squares protect the oxide underneath leaving a grid of square pillars on the substrate (see figure 2.2c). The time of etching controls the height of the pillars. When the proper height is achieved a short dip in a potassium iodide etch removes the remaining gold.

Now that we have pillars, the next step is to evaporate gold catalyst onto the sides of the pillars. As an aside, gold has multiple uses in the fabrication process. First it is used as an etch–stop for the RIE etching process. Throughout the process

gold pads surrounding the structure are used as alignment marks for the lithography process. Now we use gold as a catalyst for SiNW growth. To accomplish the catalyst evaporation we mount the sample in the thermal evaporation chamber at a steep angle (so that the *side* of the sample—and therefore the sides of the pillars—face the evaporation source). For this application we used a rotating sample holder and used a laser to align the sample face at a $3-5°$ angle to the source. Once the sample was properly mounted we evaporated 10–30Å of gold onto the sidewalls of the pillars. This serves as the catalyst in the SiNW growth process.

2.2 Nanowire Growth

The SiNW growth is accomplished using the vapor-liquid-solid (VLS) method. [4] After the catalyst has been deposited the sample is placed in a growth furnace at $450°$C with flowing silane gas (SiH_4) vapors. At these temperatures the thin-film gold agglomerates into catalyst beads on the sides of the pillars. The silane vapor breaks down into silicon in contact with the gold catalyst beads. Eventually the gold-silicon concentration reaches a eutectic point and the mixture liquifies. The flowing silane gas continues to contribute silicon until saturation occurs at which point a solid nanowire is ejected. By controlling the thickness of the catalyst we can limit the growth to anywhere from one to just a few nanowires per pillar. Ideally there would be one nanowire per pillar growing about 1μm in length out of the sidewall and along the substrate. Each nanowire could then be contacted on either side with source and drain electrodes and used as a transistor with the silicon substrate as a gate.

Chapter 3

Results

3.1 Oxide Pillars

Once we knew we could grow nanowires using the above process, the next step was to optimize the parameters to our purposes. Since the amount of catalyst controls the nanowire growth, that was a natural place to start. The amount of catalyst is controlled both directly—through the thickness of the gold evaporation—and indirectly— through the pillar height. Larger pillars provide more surface area for the catalyst evaporation, thereby increasing the total amount of catalyst. In order to determine the dependance of wire growth on pillar height we grew nanowires on substrates with similar gold depositions but varying pillar heights. Table one shows the results of that study. The pillar height is accurate to about 200Å on average. Taller pillars were not included because the silicon dioxide layer of this first batch of substrates was too thin. There must be enough oxide beneath the pillar to maintain electrical isolation between the devices and the substrate (see figure 1.1).

Pillar height	Total Surviving Pillars	Pillars with no wires	Pillars with one wire	Pillars with two wires	Pillars with three wires	Pillars with usable wires
1200 Å	35	15	11	4	3	3
2400 Å	24	3	11	3	4	11

Table 3.1 Comparison of nanowire growth on two different pillar heights. I logged the number of wires and number of usable wires on each pillar for both samples to compare the two. The 2400A pillars had almost 4 times the number of usable wires.

3.2   Contact Pads

For these pillar-grown nanowires to be useful in a LOC, they must be used as the channel for a transistor. The advantage of this selectively grown process is that we now have nanowires in exact positions specified by a lithography process. We can then use the same alignment marks in successive lithographies (and metal evaporations) to establish source and drain contacts on the ends of the nanowire. Figure 3.1 shows scanning electron microscope images of the steps of the process starting with the pillar and nanowire, then the nanowire with source and drain contact pads.

3.3   Nanowire Transistor

At this point the investigation is technically complete. However, since we have shown the feasibility of growing the nanowire and contacting it for use as a transistor the next logical step is to test the ensemble in its role as a transistor. In this device the substrate provides the gate voltage. Since the nanowire is insulated from the substrate by the layer of silicon dioxide, a voltage applied to the substrate will draw
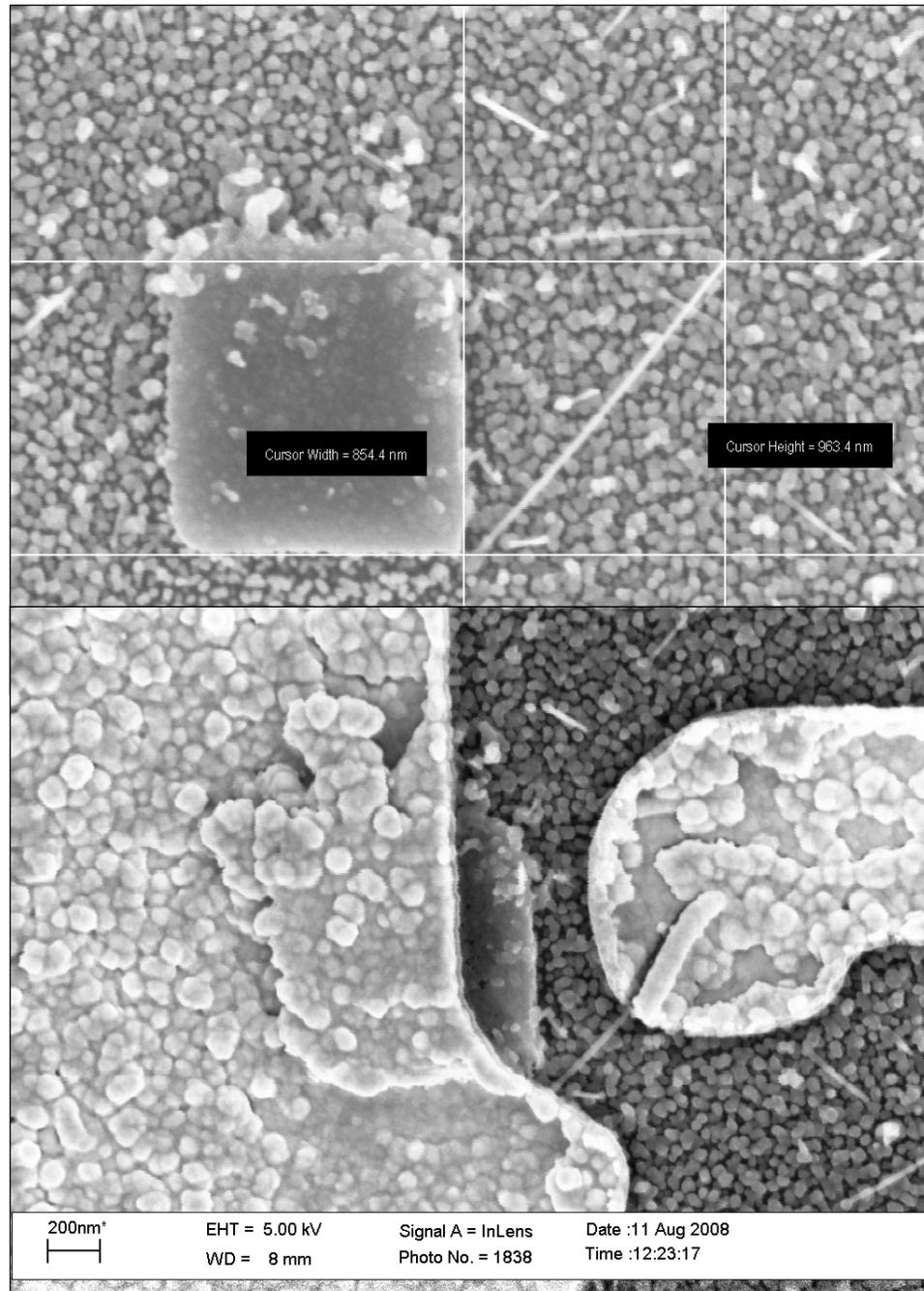
Figure 3.1 Scanning electron microscope images of the same nanowire first as grown from the pillar (top) and then after the source and drain contacts have been added. The top image gives the length of the nanowire as about 1 μm. Gold catalyst was evaporated onto the right sidewall of the pillar, resulting in the growth of this wire. The spotted surface of the substrate is the result of accumulated amorphous silicon from the nanowire growth.

charge carriers down to the bottom of the wire where they will form a conducting channel. In the eventual lab-on-a-chip the gate voltage will be applied by the ionized fluid flowing across the device, but for initial testing it was easier to use the substrate as a gate.

The first step in testing the transistor behavior of the device is to establish electrical contact with the source and the drain electrodes. Using a probe station we contacted the electrodes and applied a variable voltage across the device (with no gate voltage). The device responded ohmically with a proportional relationship between the voltage and the current (measured using a four point probe).

Once the device was contacted we were able to begin testing its transistor behavior. We applied a steady voltage across the device and measured the current through the device while applying a varying gate voltage to the substrate. The current increased slightly with increasing gate voltage as shown in figure 3.2.
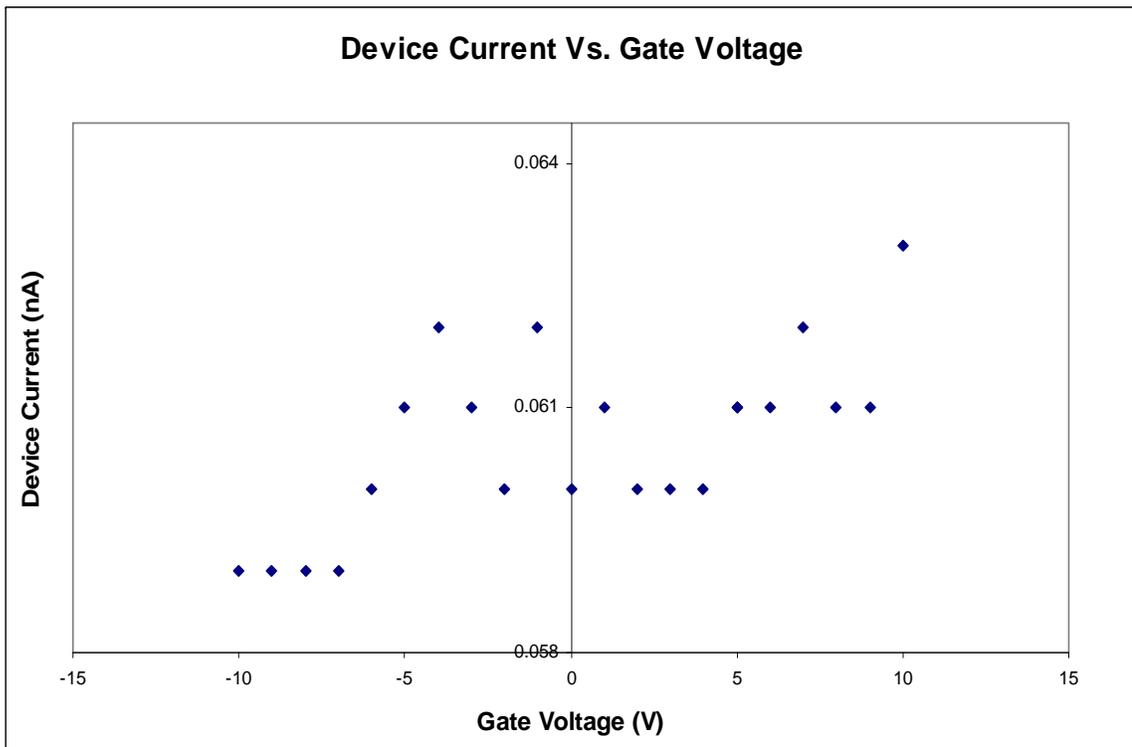
Figure 3.2 This graph shows a histogram of the device current versus gate voltage. While there was not a strict current rectification due to significant current leakage into the substrate, there was an overall tendency towards the creation of a conductive channel with higher gate voltages.

Chapter 4

Discussion

4.1 Pillars

The main goal of this project was to selectively grow silicon nanowires in such a geometry that they could be used as transistors in a NASA lab-on-a-chip sensor. This goal was accomplished by controlled placement of the SiNW catalyst. Fabrication of pillars on a silicon/silicon dioxide substrate and angle-evaporation of gold catalyst onto the sides of these pillars followed by vapor-liquid-solid deposition resulted in the growth of individual nanowires from the sides of the pillars. We found that the controllable parameters include the height of the pillars and the thickness of gold catalyst, however the pillar height is a more reliable way to control the amount of catalyst because of the exceedingly thin layer of gold($\sim$3 nm). Preliminary testing revealed that a pillar height of 2400Å produced usable nanowires on about half of the pillars.

There are several ways that this process could be refined. For one, the EBL process could be replaced by photolithography. Photolithography provides much easier alignment and repeatability of features. Once you know the patterns you want, you

can create photo-masks that will make pattern writing much easier. However this is an expensive and time-consuming task, and once a photo-mask is made, it cannot be changed. Therefore this step is best left until the rest of the process is more refined.

Another option would be to replace the square pillars with circular pillars. This would further define the location of the nanowire growth. Currently the catalyst is spread over the entire side surface of the pillar. If we used a circular pillar, the catalyst would be concentrated on the part of the circle nearest the evaporation source, with the rest of the circular side-wall forming an increasingly oblique angle with the source. This would further limit the amount of catalyst on the pillar and concentrate the catalyst at the same relative position on each circular pillar on the substrate. Furthermore this could ease the process of contacting the wires once grown because the wires might be more localized and the growth more predictable. The more limited amount of catalyst could also help avoid the occasional problem of multiple wires growing from the same pillar.

4.2 Transistors

Although it was not the main goal if this project, we successfully contacted one of the nanowires to test its behavior as a transistor. An ideal transistor exhibits a linear increase in device current with increasing gate voltage with some "cutoff voltage" where there ceases to be any current flow (see figure 4.1). In the figure the cutoff voltage is zero volts, but it could be at a positive or negative voltage depending on the amount of charge carriers in the semiconductor (the semiconductor *type* as well as the doping).

Our device showed some properties similar to an ideal transistor. A general trend of increasing device current with increasing gate voltage is certainly encouraging (see
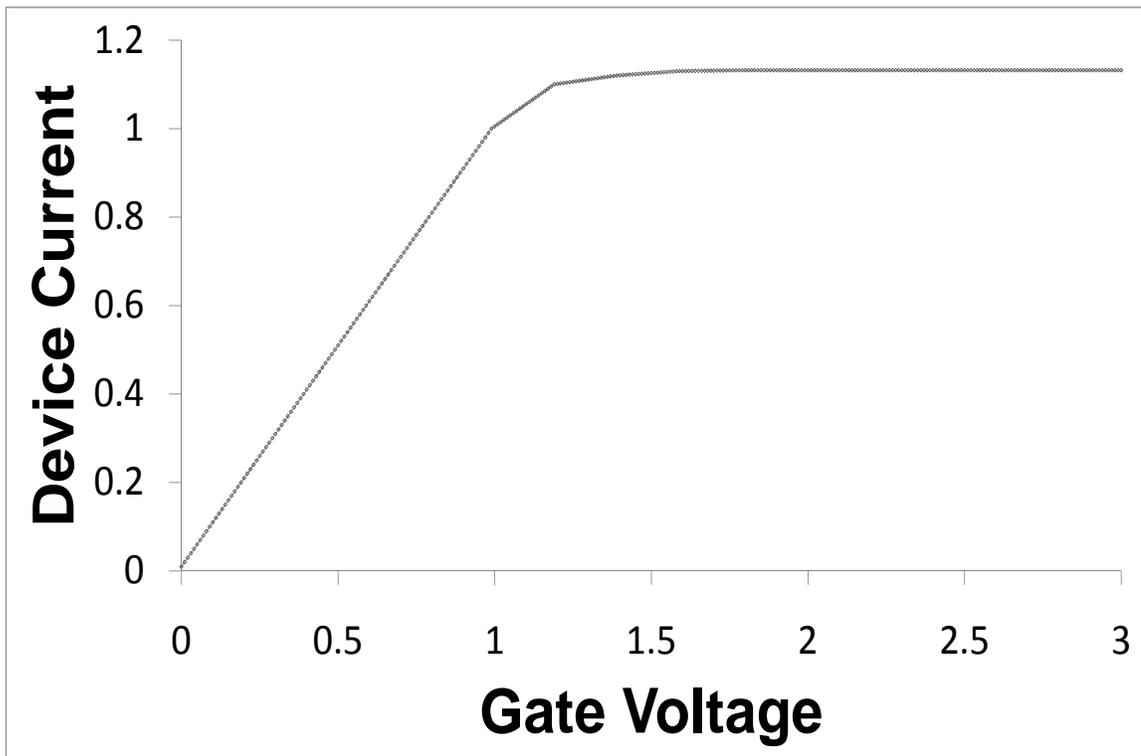
Figure 4.1 This graph shows an example of a current voltage graph for a transistor. As the gate voltage is increased the current allowed through the device increases. Eventually the conducting channel saturates and an increase in gate voltage no longer increases the current through the device (at about 1.5V in the graph).

figure 3.2 and compare figure 4.1). However, the small current increase indicates that it is not a very good transistor. Furthermore there was no indication of a cutoff voltage. This could be because the voltage was never increased enough to show the cutoff voltage (the power supply was only capable of 10 V—see figure 3.2), however the gate voltage range is quite large for a transistor.

Most likely the problems were caused by a leakage current from the device to the substrate. This could be caused by insufficient oxide thickness or defects from the fabrication process. Either way if some current supplied at the source somehow leaked to the substrate rather than the drain the semiconductor properties of the device would be compromised. The idea of a transistor relies on the charge carriers accumulating on one edge of the semiconductor channel. If there is a short to the substrate those charge carriers will not accumulate. We tested this by measuring the current from the source to the substrate. There was a small but measurable current, indicating that leakage current could be the problem.

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