Annealing of Coated Electron-Beam Induced Deposition of Platinum Nanowires

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ABSTRACT

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EBID allows metals to be directly written to a substrate in order to connect to randomly oriented devices. When depositing with the precursor $C_9H_{16}Pt$, the deposited metal has a resistivity a few orders of magnitude higher than pure platinum. Therefore, the leads are highly resistive and present problems in experimental electrical measurements. By introducing an anneal with an alumina coating, the resistivity can be lowered to $1.32\times10^{-6}\ \Omega m$, which is only 12 times above the resistivity of bulk platinum.

Keywords: annealing, electron-beam induced deposition, platinum nanowire, aluminum oxide, scanning electron microscope, photolithography, four-point measurement, contact resistance, ion beam deposition, electron beam lithography, feature size, resistivity, contact resistance

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Chapter 1

Introduction

1.1 Overview

For many decades, advances in technology have led to the creation of smaller electrical devices. In 1965, Gordon Moore predicted that each year the number of components per integrated circuit would double.[1] Since then, industry has paralleled Moore's prediction. Recently, Brian Krzanich of Intel announced that Moore's law "isn't dead" and this year (2017) Intel will release a new chip which will be both cheaper and smaller than previous chips.[2] While the industry may continue to follow Moore's law for the present time, it may soon reach a limit.

Cost and size, these are two of the leading factors in producing new devices. The smaller device is, the more expensive the equipment to manufacture it becomes. The increasing costs of the top-down approach (photolithography) may eventually "kill" Moore's now fifty-year-old prediction. However, as the world pushes towards pervasive

computing (self-driving cars, virtual reality, etc.) faster, smaller devices are needed; both industry and consumers want smaller cheaper devices to enable these, and other, technologies.

Many scientists have questioned the continued efficacy of the top-down approach. Instead, they wonder if bottom-up (or self-assembly) techniques may be better suited to build the inexpensive and smaller devices of the future. Although scientists can create billions of these self-assembled device structures simultaneously, they encounter one problem that the top-down approach lacks entirely; when placed on a surface, they do not know where the devices are nor how to connect to them. These devices are randomly organized causing major problems when using standard industrial methods to connect to them. Therefore, experiments to measure them cannot rely on industry's current techniques. To illustrate this, we will investigate photolithography, industry's leading top-down patterning tool, and then enter the realm of processes which are, or may be, used by researchers to measure self-assembled structures: electron-beam lithography, ion beam deposition, and, last of all, electron-beam deposition (EBID).

EBID, as we will explain below, is optimal for directly writing to sub nanometer features. Yet, it has a major flaw; the materials deposited by EBID have high resistivities, and therefore resistances, which are many times that of the bulk material.[3] Since highly resistive materials can prevent accurate electrical measurements, the resistivity must be reduced. We shall seek to emphasize the importance of EBID in experimentation. We shall also show that by introducing an Al_2O_3 (aluminum oxide or alumina) coating and an anneal, the resistivity of the materials deposited (using a

platinum (Pt) based precursor gas) can decrease to $1.32\times10^{-6}\ \Omega m$, which is only 12 times above the resistivity of bulk platinum.

1.2 Background

1.2.1 Optical Lithography

Optical Lithography (also known as photolithography) has dramatically improved during the last several decades.[4] Intel's employee Mark Bohr, recently announced that Intel succeeded in making 14 nm transistors.[5] While this is an amazing feat, the cost of the machinery required to produce such devices is extraordinarily high,[6] for instance, Intel pays approximately $1 billion per machine.[7] These highly advanced machines have the capability to correctly create the right-sized devices, but the cost is too high for many companies and universities. Therefore, the cost itself prevents many scientists from experimenting with connecting to bottom-up devices using this equipment.

Optical lithography allows materials to be deposited in predefined patterns registered to known features on a substrate. This limits its effectiveness in connecting to randomly oriented bottom-up devices. To illustrate its ineffectiveness, consider some of the self-assembled structures. Some of the common bottom-up microfabrication techniques result in metalized DNA (deoxyribonucleic acid),[8-10] CNT structures (carbon nanotubes).[11] Let us figuratively attempt to attach to Pearson, et al.'s metallized DNA structure; dimensions of approximately 150 nm long and 5 nm in diameter.[9] Most university and research lab equipment (to perform photolithography) is limited to ~2 μm resolution for contact lithography or ~0.2 μm for projection lithography. This means that

the research photolithography tools currently in use are incompatible with making electrical contacts to these self-assembled nanostructures.

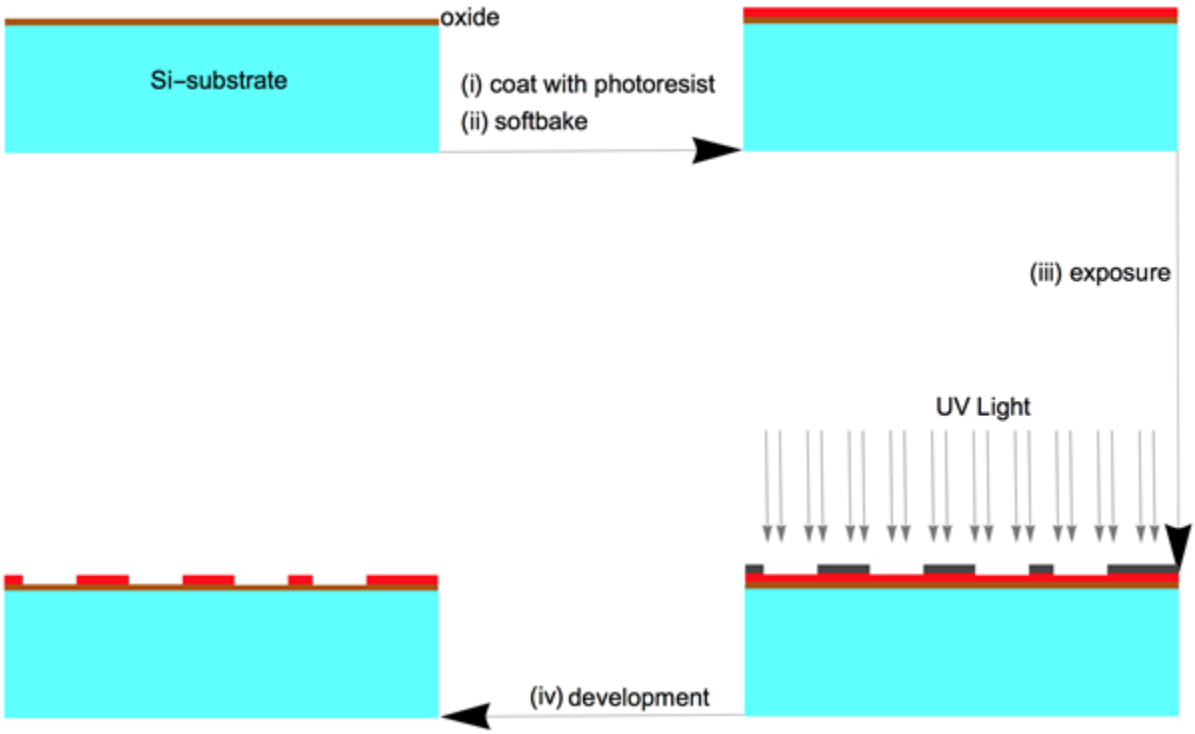

Figure 1.1. Steps of photolithography (i) spin on photoresist (ii) heat substrate to harden resist (iii) cover sample with a mask and shine ultraviolet light to expose resist (iv) the developing step, when immersed in a basic solution, removes the exposed resist.

1.2.2 Electron-Beam Lithography

Electron-Beam Lithography (EBL) can be used to create patterns that have sub 5 μm features. Because of the slow write speeds, this results in high costs for large scale industrial fabrication of devices, but EBL is ideal for prototyping, making masks, and experimentation.[12] EBL utilizes a SEM (scanning electron microscope) or a similar machine. EBL, like photolithography, exposes the resist via an electron beam rather than UV light.

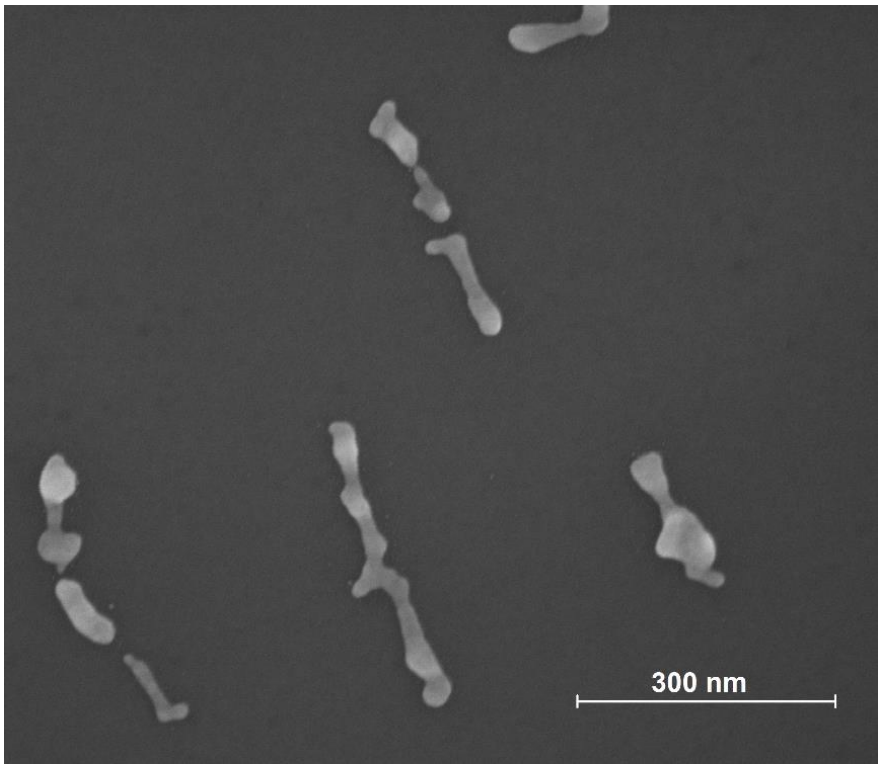

Figure 1.2. SEM image of plated DNA origami structure. DNA is deposited at random locations on various parts of the substrate.

Again, let's try to figuratively connect to Pearson et al.'s metallized DNA[9] (see Figure 1.2). The metallized DNA were mixed in a solution and then the solution was placed on a surface, an oxidized silicon substrate. While in the solution, the metallized DNA would have been relatively mobile, then, when placed on the substrate, Van der Waals forces would have attracted the DNA to a random location on the substrate.

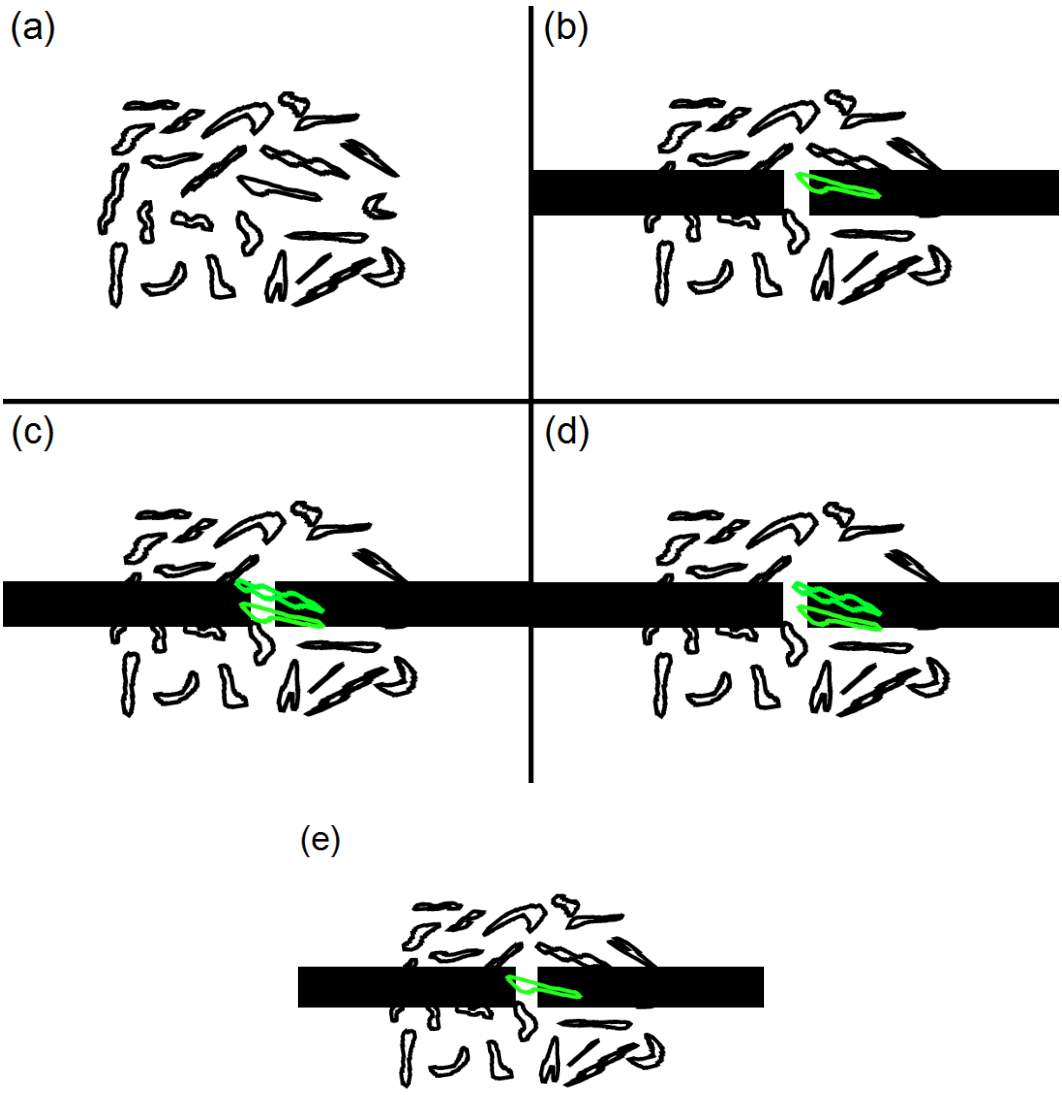

Figure 1.3. The metallized DNA that will are connected to in this illustration are green (structures are placed on top of lead to allow easy identification), the leads are the black rectangles. (a) metallized DNA, (b) two-point measurement where leads are covering desired, (c) two-point measurement where leads connect to multiple structures (d) the most case, leads cover multiple structures but connect to none. (e) multiple structures covered but one connects.

To measure one individual metallized DNA, the electrodes must connect to only one strand (see Figure 1.3). Pearson sought to avoid connecting to multiple strands by

creating an array of electrodes (see Figure 1.4 for details). In the event that multiple strands were connected, he may have assumed that each strand had approximately the same resistivity. From there, he may have calculated the resistivity for one strand. This, however, presents a problem that arises from two-point measurement (two-point and four-point measurements are discussed later).

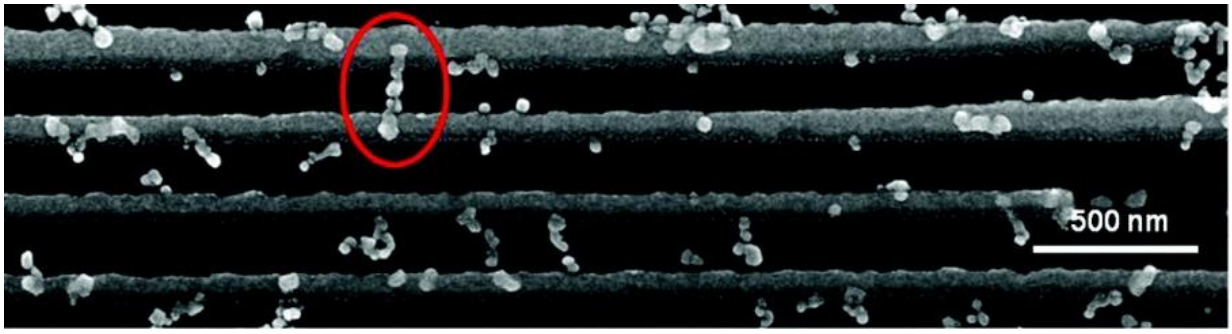

Figure 1.4. SEM image of EBL nanostructures. The structures, when created, come into contact with many strands of metallized DNA. The strand circled in red represents one strand where a connection is made. However, the structure may connect to other strands simultaneously. Cropped figure is used with permission: A.C. Pearson, E. Pound, A.T. Woolley, M.R. Linford, J.N. Harb, and R.C. Davis, Nano Letters 11, 1981 (2011).

Besides the problems relating to connecting to the structures, the electron-beam itself may cause further problems. When the electron beam interacts with the resist and substrate, the electrons scatter. McCord & Rooks[13] explain that the secondary electrons (electrons that only penetrate a few nanometers before being scattered back to the surface) expand the beam diameter by 10 nm. Between the secondary electrons and backscattered electrons (the electrons that are scattered back through the resist a

second time), the proximity effect exposes the resist in nearby areas thereby limiting the minimum device size.[13,14]

1.2.3 Ion Beam Deposition

Since the 1980s, ion beam induced deposition (IBID) has become more widely used in research laboratories.[15] IBID is a process that, in many ways, is complementary to EBL and photolithography. IBID and EBID are both direct write methods (see Figure 1.5 for a brief description of how these processes work) and, although the beam type changes, the methods themselves have many similarities. Generally, the deposited material is conductive, and, in both IBID and EBID, the material can be used to form many versatile structures for instance nanowires,[16] and electrical contacts to carbon nanotubes.[17]

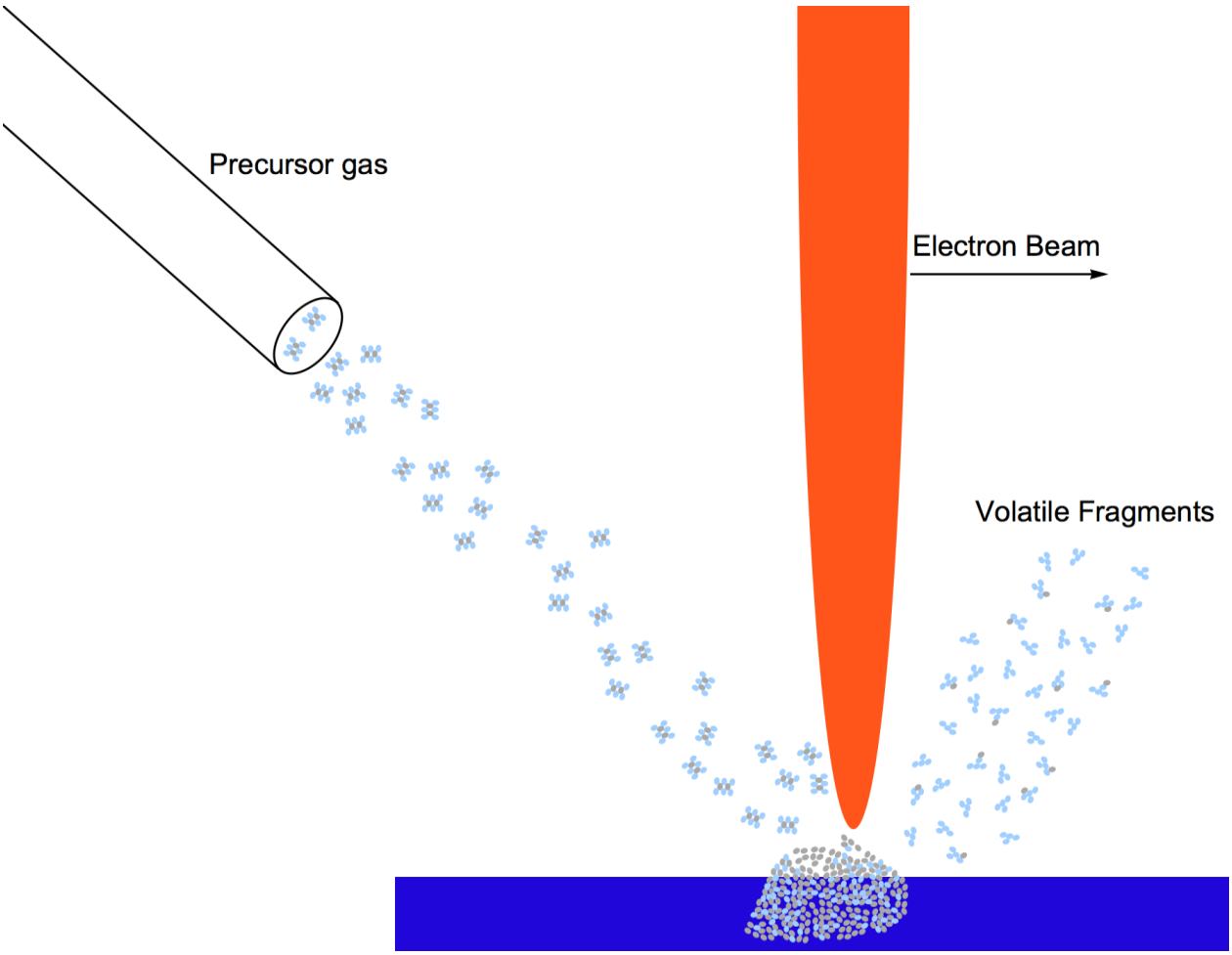

Figure 1.5. A precursor gas is in injected into a chamber held at high vacuum. There, the gas interacts with a beam (electron or ion). The beam separates the gas into two components, volatile and nonvolatile.[18] The volatile components are then pulled out of the system leaving the deposited nonvolatile component. The beam scans the surface causing the metal to deposit in a controlled pattern.

Makarov & Jain[19] found that IBID over-sprays the target area with a conductive material that may cause shortages in close proximity electrical devices. Vladov, Segal, & Ratchev[20] noticed that IBID has trouble writing 19 nm sized devices. Chen, et al.,[21] discovered that backscattered gallium ions appeared 10 μm away from the beam causing a thin Pt deposit. Backscattering is a major issue in IBID on the nanoscale.

1.2.4 Electron-Beam Induced Deposition

EBID is not commonly used in connecting to randomly oriented devices. EBID does not suffer the same levels of backscatter deposition experienced by IBID. EBID, however, leaves deposits with highly impure material.

A typical material deposited by EBID is Pt (commonly deposited with Trimethyl(Methylcyclopentadienyl)Platinum(IV) ($C_9H_{16}Pt$) as the precursor gas). Langford, Want, & Ozkaya[22] observed that IBID, when writing with a precursor gas containing Pt, deposits a material with a resistivity much lower than that of EBID's Pt deposits. Experiments performed by Botman, Hesselberth, & Mulders,[23] Botman, Mulders, & Hagen,[24] Dorp, et al.,[25] Mulders,[18] and Mulders, Belova, & Riazanova,[26] have shown that the material deposited by Pt precursor gases tend to leave a material with a resistivity many times larger than that of the bulk material. EBID structures contain both Pt and large percentages of carbon (up to 80%).[3, 27]

In comparison to IBID, EBID damages the substrate less and has higher resolution.[28] Advantages aside, EBID cannot efficiently be used in experiments because of the high carbon content in the deposit. Therefore, the deposit must be purified for many practical uses.

1.2.5 Two-point Measurement

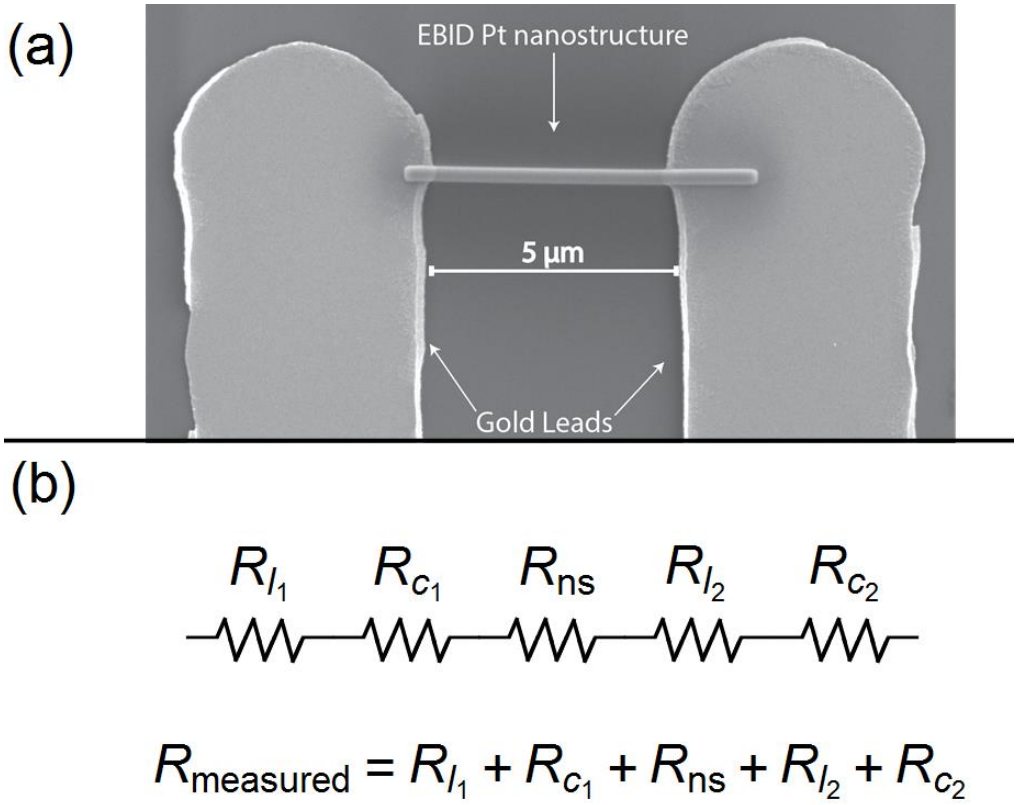

Figure 1.6. The two-point measurement (a) involves a current is sent through the lead and a voltage is measured (b) in taking a two-point measurement, the desired resistance is the resistance of the nanostructure (R_{ns}), but the measured resistance will include the resistances of both leads (R_{l_1}, R_{l_2}) and the points of contact (R_{c_1}, R_{c_2}) between the nanostructure and the leads.

In all electrical measurements, there are at least two sources of resistance: resistance inherent in the materials and resistance in the contact between the materials.[29] In the two-point measurement, the resistance measured is the sum of these types of resistance (see Figure 1.6). While the resistance of the nanostructure is desired, the resistance of the all components involved influences the outcome. But this can easily be eliminated through the four-point measurement.

1.2.6 Four-point Measurement

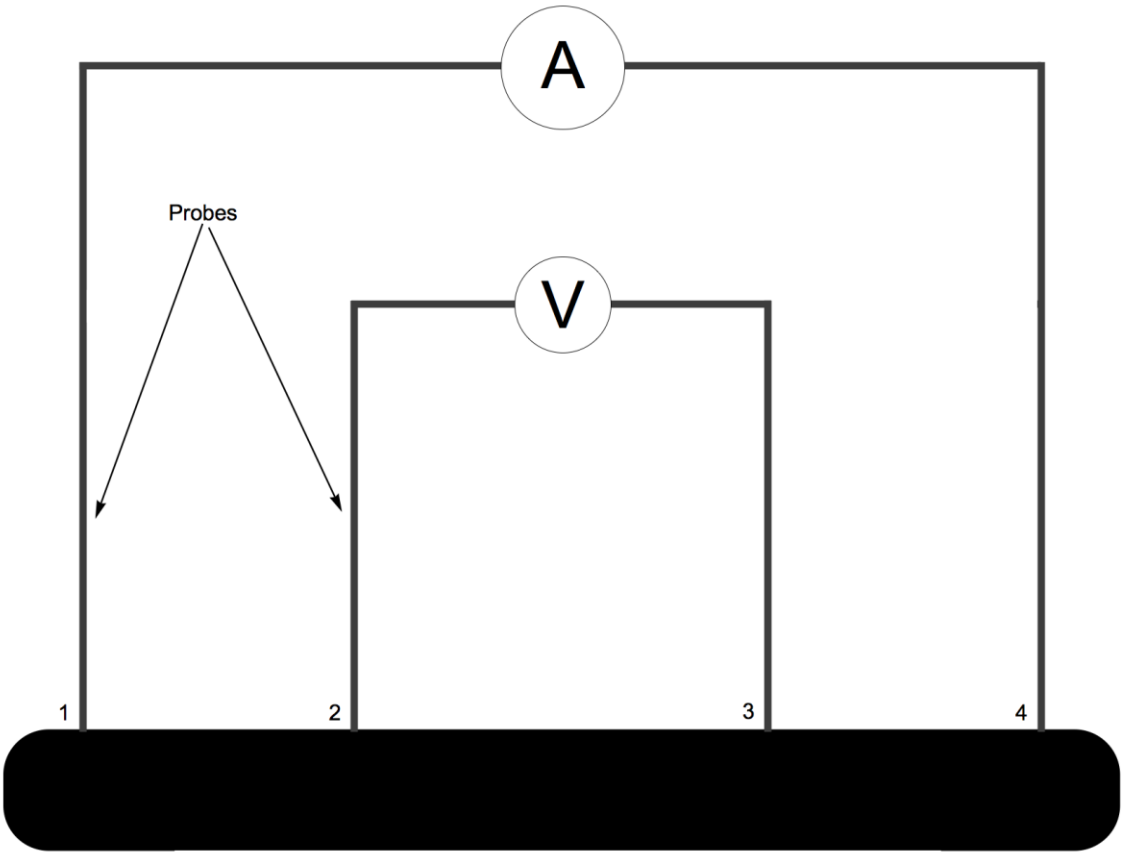

Figure 1.7. A constant current is sent through probes 1 and 4. Probes 2 and 3 are connected to the section of material which shall be measured. Through probes 2 and 3 a voltage is measured.[30] Once a voltage is measured, the resistance of the material can be calculated via Ohm's Law.

The four-point measurement (Figure 1.7) allows us to isolate the resistance of the structure under test from the resistance of the measurement leads. Because of the impurities in the material deposited by EBID, a four-point measurement must be made.

This, however, only provides an accurate resistance if the resistance of the measured structure is much smaller than the internal resistance of the voltmeter. If the

structure's resistance is too high, an appreciable current travels through the voltmeter so the leads to the voltmeter. If the internal resistance of the voltmeter is much greater than the sample's resistance, then, according to equation 1.1, I_2 is much less than I_1. This means that the other resistances negligibly influence the voltage measured. The resistance in EBID Pt deposits (which typically are on the order of 10^7 Ohms) will be too large for accurate four-lead measurements to be made. Consequently, the resistivity of the EBID deposits must be reduced.

Equation 1.1. Characterization of four-point measurement resistance and voltmeter. Specifically, how the voltmeter perceives the resistances.

$$V_{voltmeter} = I_1 R_{sample} + I_2(R_{contact\ resistance} + R_{test\ leads})$$

1.3 Annealing

One method of reducing the resistance of the deposit is by introducing an anneal post-deposition. Botman, et al.,[24] Mulders et. al,[26] have shown that annealing has been shown to burn off CO or CO_2 from EBID Pt nanowires leaving behind Pt of a much higher purity.

1.4 Annealing of Coated EBID Nanostructures

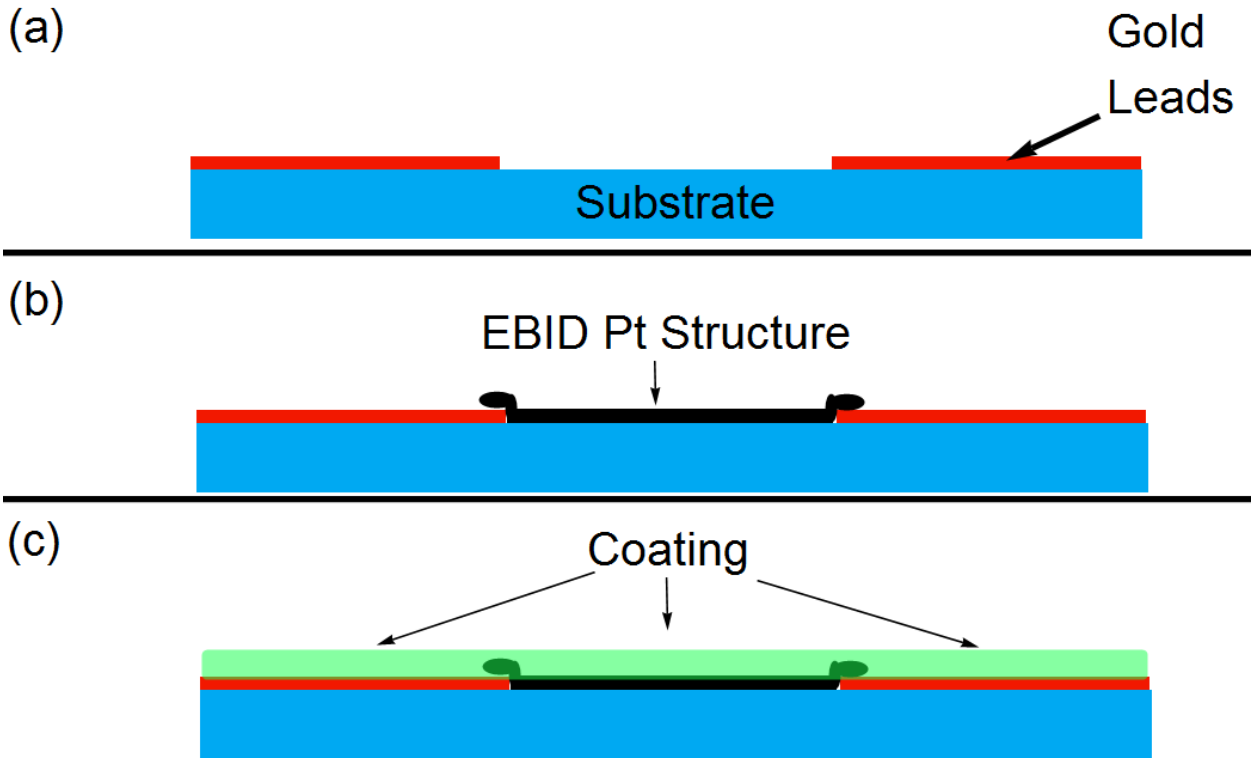

Figure 1.8 The following is a diagram of investigation. (a) photolithographically defined gold leads (b) EBID Pt Structure (c) coating (either of ZEP 520A or alumina)

As has been previously studied, annealing EBID structures can significantly lower resistivity, enabling nanostructure electrical measurements. However, our research team has observed that annealing of metal nanostructures causes significant morphological changes—even damage to the structure. An anneal, as low as 200℃, of a metallized DNA nanowire will cause the metal wire to bead up and completely lose any conductivity. By putting a thin polymer coating over metal nanostructures, prior to annealing, the structures retain their shape and their conductivity actually improves. Electrical measurements can now be performed on the metal nanostructures since they

remain intact after annealing. Using EBID, we can connect to the metal nanostructures. However, to measure the metal nanostructures, the EBID structures must be coated with the same polymer (Figure 1.8). How the polymer interacts with the EBID deposit's resistivity is unknown. Here we will investigate the impact of annealing on the resistivity of EBID nanostructures that have been coated with ZEP 520A and of Al_2O_3. We will also study the influence of the coated structure's height on its resistivity.

Chapter 2

Materials and Methods

2.1 Materials

HMDS (Hexamethyldisilazane) and NMP (M790603-4L Lot # SHBG9647V) were purchased from Sigma-Aldrich. The photoresist AZ 3312 and the AZ300MIF were obtained from IMM (Integrated Micro Materials). The ZEP 520A was procured from Zeon Chemicals. The chromium plated tungsten rod (P/N: CRW-2) and gold (P/N: RDM-WBAO) crucibles used for evaporation were purchased from R.D. Mathis Company. The gold shot used in the crucible was 99.99% pure and came from Refining Systems Inc.

2.2 Methods

2.2.1 Wafer Preparation

2.2.1.1 Photolithography

4” silicon wafers, with approximately 80 nm of Al_2O_3 deposited by e-beam evaporation, were broken into approximately $1\ cm^2$ sized pieces. After cleaning the samples in purified water, HMDS is then spun on at 2000 rotations per minute (rpm) for four seconds (using a Laurell Spin Processor WS-400A-6NPP-LITE). Immediately following this AZ 3312 is spun on at 4000 rpm for 60 seconds which leaves a coating approximately 1 μm thick. Following a soft bake (90℃ for 60 seconds on a hot plate), the samples were then put in contact with a mask and exposed to UV light with a mask aligner (Karl Suss MA 150). To develop the resist, the samples are submerged in AZ300MIF for 20-25 seconds, then they are cleaned by rinsing them in purified water and dried via using a stream of nitrogen.

2.2.1.2 Thermal Evaporation of Gold

2.2.1.2.1 Deposition

Using a BYU custom made Thermal Evaporator the chromium and gold were evaporated to the sample. Samples were placed in a vacuum with two crucibles: one containing chromium and the other gold. Once the chamber reached high vacuum a current was put through the chromium containing crucible and 7 nm were thermally deposited. Following the chromium deposition, 50 nm of gold were deposited.

2.2.1.2.2 Lift Off

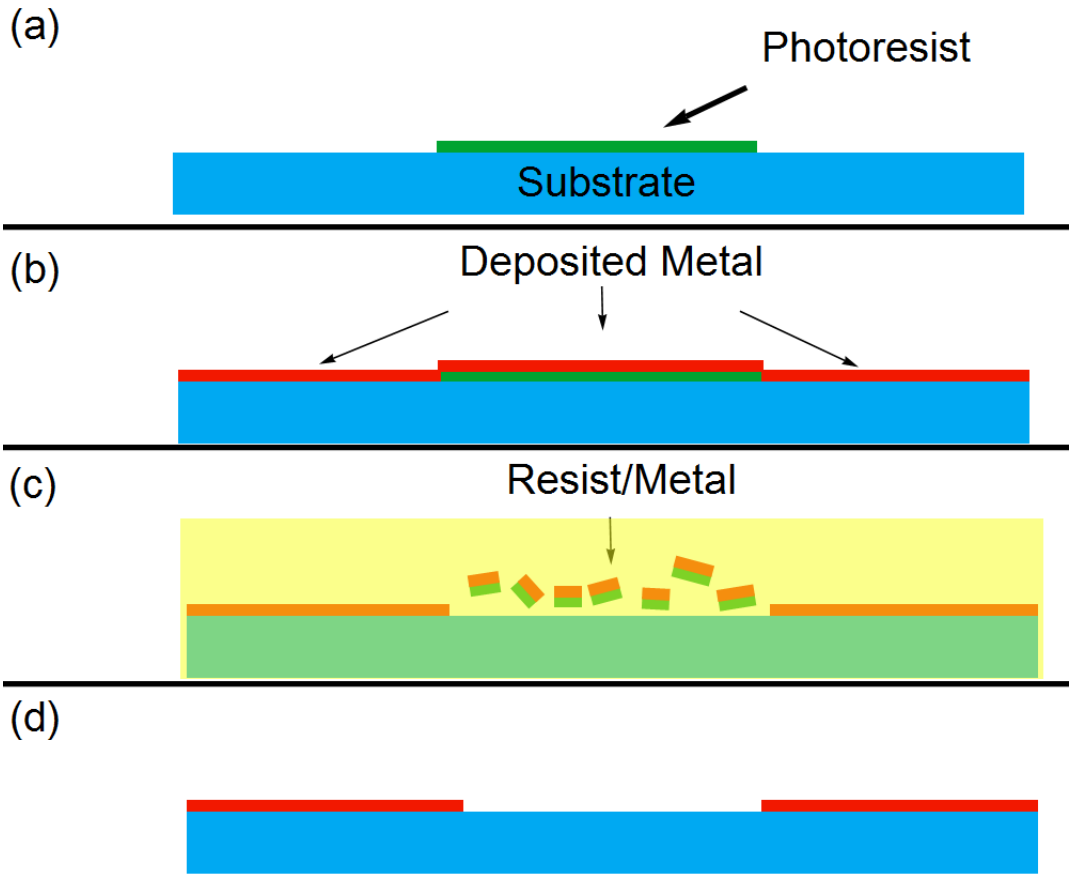

Figure 2.1 (a) Photoresist is photolithographically defined. (b) A metal is deposited onto a substrate; the metal completely covers the substrate and resist. (c) substrate is immersed in a chemical (the type of chemical depends on the specific resist) solution that dissolves the patterned resist and the metal on top of the resist comes off as it is dissolved. In some cases, the substrate/chemical solution will be sonicated to assist in dislodging the resist (d) the process ends with the metal in every place the resist was not.

To remove the resist and the excess metals (Figure 2.1), the samples were put in NMP (n-methyl-2-pyrrolidone) and sonicated for 5 minutes. The samples were then cleaned by rinsing in purified water and dried with a stream of air.

2.2.2 EBID Nanowires

To write the EBID nanowires, a Helios Nanolab 660 DualBeam by FEI was used. Beam voltage was set at 5 kV with a spot size of 0.17 nA. Before inserting the precursor, $C_9H_{16}Pt$, FEI's gas injection system was sent into the SEM's chamber. The precursor source was set to a "warm" (a predetermined temperature by FEI). The dimensions of the written EBID structures were 250 nm in the z-direction, 200 nm in the x-direction, and 3 μm in the y direction. The structures that connect to this measured wire vary in length but connect to gold leads such that a four-point measurement can be made. Each sample had between 3 to 10 structures.

2.2.3 Coating Nanowires

2.2.3.1 ZEP 520A

Using a spinner, the 1 mm of ZEP 520A (ZEP) was spun onto each sample. Then the ZEP was baked at 200℃ for 2 minutes. (The time used to bake the ZEP to the sample was included added to the annealing time.) Following annealing the samples, the ZEP was removed. In order to remove the ZEP, the samples were submerged in NMP for times between 15 minutes to 24 hours. The samples were then rinsed in purified water and dried with a stream of nitrogen.

2.2.3.2 Aluminum Oxide

Using a Denton Vacuum E-Beam Evaporator approximately 100 nm of Al_2O_3 were deposited on each sample. 2.2.4 Annealing

2.2.4.1 Planar Etch 2 Plasma Etcher

Samples were loaded into the chamber and put under vacuum (above 100 mTorr). The samples were then exposed to an oxygen plasma. The plasma was set at a power of 55 to 73 W. Every sample was exposed for 20 seconds.

2.2.4.2 Thermolyne 6000 Furnace

The furnace was preheated to a temperature between 200℃ to 400℃. Two experiments were performed (however, there was no between the two). In one case, the samples were placed on room temperature glass before placing them in the furnace. In the other case, the samples were placed on preheated glass inside the furnace.

2.2.5 Electrical Measurements

Pre-annealing and post-anneal electrical measurements were made using a LabVIEW VI and micromanipulators. In the following experiments all that was required to take the measurements was touching the micromanipulators to the appropriate sections of the sample and a constant current (about 10^{-10} Amperes): standard annealing, oxygen plasma anneal, and anneal with the ZEP (in this case the ZEP was removed before measuring). However, after depositing the alumina we had to partially scrape off the alumina in order to take the measurements.

Chapter 3

Results and Conclusion

3.1 SEM Image of EBID Structures

The SEM image in Figure 3.1 illustrates how the EBID Pt wires connect to the photolithographically defined gold leads. We will present our results first with the uncoated annealed wires, and then move to the coated annealed wires.

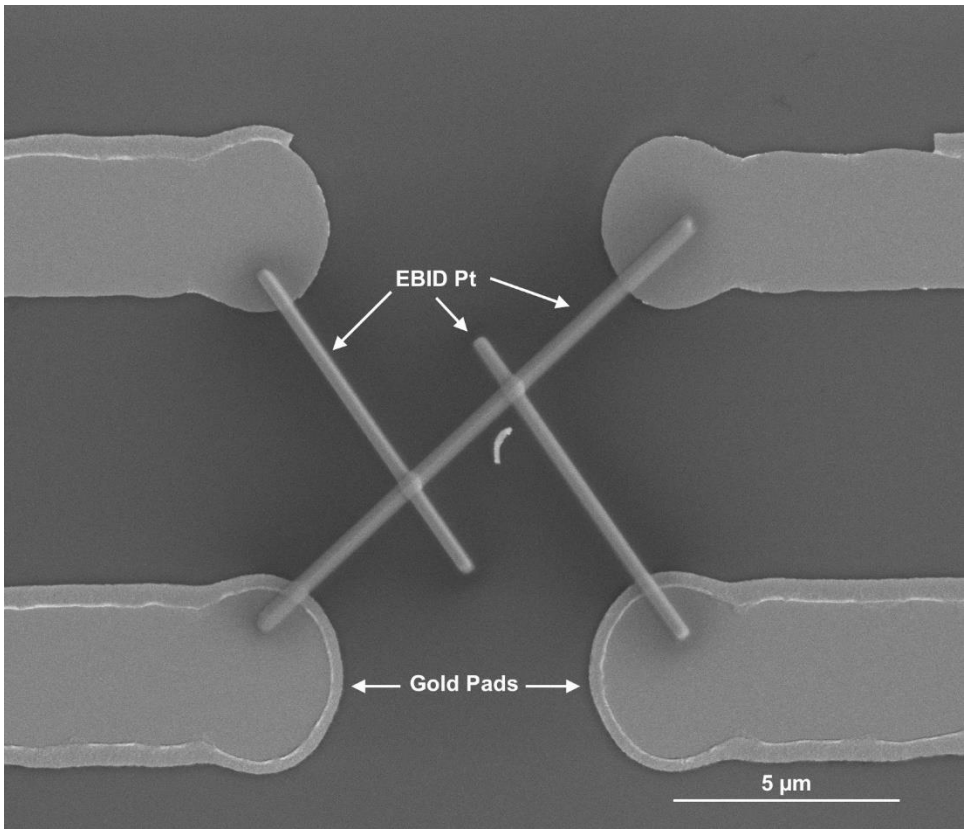

Figure 3.1 SEM image of EBID Pt structure connecting to gold leads.

3.2 Electrical Measurement of EBID Pt Nanowires

After writing the Pt nanostructures, the gold leads were put in contact with micromanipulators. Then a LabVIEW VI controlled the constant current, and changed the voltage for every measurement. (Specifically, the VI took 20 data points per measurement. The first data point started at a chosen voltage and then, for each successive data point, the VI increased the voltage. Rather than continuously increasing the voltage, it stepped up the voltage—$V_{step} = \frac{V_{max}}{n+1}$ where n represents the number of steps—until it hit a maximum voltage. It then stepped down until arriving at the original voltage). When completing the measurement cycle, the VI calculated the

maximum resistance of the wire based on the largest measured voltage. The as written Pt wires had a resistance on the order of 10^7 Ohms.

3.3 Annealing Methods Studied

3.3.1 Furnace Annealing

Table 1 shows the electrical measurements of the EBID annealed samples. The two different types of measurements (preheated surface and tepid surface) did not reveal any significant difference in the resistivities of the uncoated EBID wires.

Table 1. Comparison of the EBID deposit's resistivity before annealing (untreated) to after.

Beam Voltage (kV)	Heating*	Measurement Type	Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Temperature (°C)	Time (min)
10	None	Four-point	4.83×10^{-2}	3.40×10^{-2}	200	10
5	Pre	Four-point	3.15×10^{-2}	1.09×10^{-1}	300	2
5	None	Two-point	1.97×10^{-2}	6.28×10^{-2}	200	8
5	None	Two-point	3.95×10^{-2}	3.20×10^{-2}	200	4
5	None	Two-point	1.17×10^{-1}	4.38×10^{-2}	100	4
5	None	Two-point	5.92×10^{-2}	2.72×10^{-2}	100	4
5	Pre	Two-point	3.27×10^{-2}	5.22×10^{-2}	200	4

*Refers to the surface the sample was placed on at the start of the anneal. *Pre* means the surface on which the sample was placed was at the temperature of the furnace prior to setting the sample atop. *None* indicates that the surface on which the sample was placed was at room temperature prior to the anneal.

3.3.2 Plasma Etcher

The oxygen plasma caused the resistivity in the platinum leads to decrease (Table 2), however a closer study indicated that the plasmas interaction caused more than that. Since oxygen plasmas are often used to clean wafers to remove organic layers, it was very much unexpected to find that both the EBID structures and gold leads were partially removed during the anneal. Exactly how the plasma changed the resistivity platinum is unknown.

Table 2. Oxygen plasma anneal.

Power (Watt)	Beam Voltage (kV)	Measurement Type	Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Time (min)
56	5	Four-point	2.05×10^{-1}	2.55×10^{-2}	2
73	5	Four-point	2.77×10^{-2}	2.48×10^{-2}	2

3.3.3 ZEP 520A Coating

We believe that applying the e-beam resist successfully assisted in maintaining the EBID structures during the annealing phase. However, nearly half of the samples (and at least one wire per sample) exhibited signs that the annealing actually caused an increase in the resistivity rather than decreasing it (Table 3). Therefore, it is suspected that there may have been an unexpected chemical reaction that reversed the desired effect.

Table 3. Comparison of samples coated with ZEP before anneal. Each wire was written with a beam voltage of 5 kV

Time (min)	Measurement Type	Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Temperature (°C)
2	Two-point	1.97×10^{-2}	1.72×10^{-2}	200
2	Two-point	2.22×10^{-2}	1.75×10^{-2}	200
4	Two-point	1.72×10^{-2}	2.73×10^{-2}	200
4	Two-point	7.95×10^{-2}	1.08×10^{-1}	200
6	Two-point	2.90×10^{-2}	2.77×10^{-2}	200
8	Two-point	2.80×10^{-2}	7.28×10^{-2}	200
12	Two-point	1.43×10^{-1}	2.82×10^{-2}	200

3.3.3.1 ZEP with Varied Wire Heights

This particular experiment accentuates the effect of the ZEP discovered in the previous test. Changing the wires' height did not decrease the resistivity in any noticeable fashion (Table 4). It is possible that the height can influence the resistivity of the electrodes, further experimentation is necessary.

Table 4. Samples, with varied wire heights, coated with ZEP before annealing resulted with resistivities similar to those not annealed or with badly deposited EBID nanowires.

Z Height (nm)	Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Temperature (°C)	Time (min)
100	7.95×10^{-2}	1.08×10^{0}	200	4
300	1.24×10^{-1}	2.34×10^{0}	200	4
300	2.98×10^{-2}	6.15×10^{-1}	200	4
350	2.52×10^{-2}	5.63×10^{-1}	200	4

3.3.4 Aluminum Oxide Coating

The evaporated Al_2O_3, like the ZEP, successfully held the gold leads in place. Generally, as shown in Table 5, the resistivity dropped a few orders of magnitude. Only four samples were tested with alumina, but based on the limited data gathered it seems that annealing around 400℃ may be the optimal temperature.

Table 5. The approximately 100 nm of Al_2O_3 contributed to the resistivities of the EBID Pt nanowires to drop close to that of bulk platinum. Because of the significant changes, this table includes a comparison of resistivities to assist in explaining my conclusions.

Time (min)	Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Temperature (°C)
4	3.51×10^{-2}	1.44×10^{-3}	200
4	8.20×10^{-3}	5.96×10^{-6}	400
6	1.11×10^{-2}	1.32×10^{-6}	400
6	5.83×10^{-2}	4.41×10^{-2}	200

3.4 Conclusion and Outlook

In conclusion, the samples, coated with a layer of Al_2O_3, and annealed at 400℃ exhibited resistivities on the order of $10^{-6}\ \Omega m$. In comparison, the resistivity of bulk platinum is $10.6\times10^{-8}\ \Omega m$. This means that annealing with alumina decreased the resistivity to only 200 (in one case 12) times larger than bulk platinum. The lower resistivity puts nanostructure resistances into the kΩ range. Resistances of this order are small compared to the internal resistance of voltmeters.

Annealing with alumina brought the resistances of the wires low enough for them to be used in measuring nanodevices. Granted, the devices created must undergo several minutes of annealing at ~400℃. At any rate, we have shown that it is possible to decrease the resistivity of EBID devices.

Admittedly, there might be changes in the metallized nanostructures, although the significant change in resistance may indicate otherwise. This raises interesting questions regarding the nature of annealing thin gold structures and the nature of the contact between the EBID electrodes and the gold leads.

Appendix A

All Results

To provide the reader with all information regarding all the experiments. The following tables represent every studied method of annealing. It comprehensively covers the data gathered. Each row represents an electrical measurement made on a unique wire. There are columns to indicate the measurement type to clarify. Unless indicated otherwise, the beam voltage is 5 kV.

Table A.1. This table represents of the first measurementsmade. The wires were untreated (not coated). The measurement was a two-point measurement and the surface was not preheated. The wire here was made using a beam voltage of 10 kV.

Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Temperature (°C)	Time (min)
4.83×10^{0}	3.40×10^{-1}	200	10

Table A.2. The wires here we untreated. The electrical measurements were made with a two-point measurement. The surface was not preheated prior to the anneal.

Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Temperature (°C)	Time (min)
1.39×10^{-1}	5.07×10^{-2}	200	4
3.27×10^{-2}	5.22×10^{-4}	200	4

Table A.3. The wire here was untreated. The electrical measurements made were four-point measurements. The surface was not preheated. The wire here was made using a beam voltage of 10 kV.

Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Temperature (°C)	Time (min)
3.15×10^{-1}	1.10×10^{-1}	300	2

Table A.4. The wires here were untreated. The electrical measurements were two-point measurements. Beam voltage was 5 kV.

Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Temperature (°C)	Time (min)
3.42×10^{-2}	2.87×10^{-2}	200	4
3.95×10^{-2}	3.20×10^{-2}	200	4
5.92×10^{-2}	2.72×10^{-2}	100	4

6.18×10^{-2}	5.53×10^{-2}	100	4
9.17×10^{-2}	5.00×10^{-2}	100	4
1.01×10^{-1}	5.43×10^{-2}	100	4
1.83×10^{-1}	5.93×10^{-1}	200	4
5.87×10^{-1}	1.23×10^{0}	200	4
1.17×10^{0}	4.38×10^{-2}	100	4
7.37×10^{-1}	9.27×10^{-1}	200	8
1.27×10^{0}	5.52×10^{-2}	200	8
1.97×10^{1}	6.28×10^{-1}	200	8

Table A.5. This sample was untreated. After an initial anneal, the samples that were reannealed. The electrical measurements were made through a four-point measurement. The surface was not preheated. The wire here was made using a beam voltage of 10 kV.

Resistivity (untreated, Ωm)	**Resistivity (annealed, Ωm)**	**Temperature (°C)**	**Time (min)**
4.77×10^{0}	5.87×10^{-2}	200	10

Table A.6. These samples were untreated. After an initial anneal, the samples that were reannealed. The electrical measurements were made by a two-point measurement. The surface was not preheated.

Resistivity (untreated, Ωm)	**Resistivity (annealed, Ωm)**	**Temperature (°C)**	**Time (min)**
3.95×10^{-2}	5.07×10^{-2}	200	4
3.42×10^{-2}	7.85×10^{-2}	200	4
1.83×10^{-1}	5.12×10^{0}	200	4
1.25×10^{0}	2.00×10^{-1}	200	8
7.37×10^{-1}	1.33×10^{1}	200	8
2.0×10^{1}	2.87×10^{1}	200	8

Table A.7. The wires here were untreated and were annealed by the Plasma Etcher.

Power (Watt)	Measurement Type	Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Time (min)
56	Four-point	2.05×10^{-1}	2.55×10^{-2}	20
73	Four-point	6.63×10^{-2}	6.27×10^{-2}	20
73	Four-point	2.77×10^{-2}	2.48×10^{-2}	20

Table A.8. In this experiment, the wires were coated with ZEP 520A and the wire heights changed. The samples were annealed on a hotplate.

Z Height (nm)	Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Temperature (°C)	Time (min)
100	7.95×10^{-2}	1.08×10^{0}	200	4
300	1.24×10^{-1}	2.34×10^{0}	200	4
300	2.98×10^{-2}	6.15×10^{-1}	200	4
350	2.52×10^{-2}	5.63×10^{-1}	200	4

Table A.9 The wires here were coated with ZEP 520A prior to the anneal.

Measurement Type	Resistivity (untreated, Ωm)	Resistivity (annealed, Ωm)	Temperature (°C)	Time (min)
Two-point	3.32×10^{-2}	3.51×10^{-2}	2	200
Two-point	1.97×10^{-2}	1.71×10^{-2}	2	200
Two-point	2.08×10^{-2}	1.87×10^{-2}	2	200
Two-point	2.36×10^{-2}	2.16×10^{-2}	2	200
Two-point	5.32×10^{-2}	1.24×10^{-1}	2	200
Two-point	3.09×10^{-1}	1.77×10^{0}	2	200
Two-point	2.22×10^{-2}	1.76×10^{-2}	2	200

Two-point	6.77×10^{-2}	1.90×10^{-1}	2	200
Two-point	2.97×10^{-2}	3.10×10^{-2}	2	200
Two-point	3.02×10^{-2}	3.81×10^{-2}	2	200
Two-point	1.22×10^{-1}	1.06×10^{0}	4	200
Two-point	5.75×10^{-2}	3.43×10^{-1}	4	200
Two-point	1.76×10^{-2}	3.03×10^{-2}	4	200
Two-point	8.84×10^{-2}	7.91×10^{-1}	4	200
Two-point	1.71×10^{-2}	2.73×10^{-2}	4	200
Two-point	1.91×10^{-2}	3.58×10^{-2}	4	200
Two-point	1.24×10^{-1}	2.36×10^{0}	4	200
Two-point	2.51×10^{-2}	5.64×10^{-1}	4	200
Two-point	2.99×10^{-2}	6.16×10^{-1}	4	200
Two-point	7.95×10^{-1}	1.08×10^{0}	4	200
Two-point	3.35×10^{-2}	4.26×10^{-2}	6	200
Two-point	3.08×10^{-2}	3.61×10^{-2}	6	200
Two-point	4.30×10^{-2}	7.41×10^{-2}	6	200
Two-point	2.89×10^{-2}	2.76×10^{-2}	6	200
Two-point	4.26×10^{-2}	8.75×10^{-2}	6	200
Two-point	4.95×10^{-2}	1.64×10^{-1}	6	200
Two-point	4.59×10^{-2}	1.64×10^{-1}	8	200
Two-point	3.13×10^{-2}	8.67×10^{-2}	8	200
Two-point	4.88×10^{-2}	1.77×10^{-1}	8	200
Two-point	2.59×10^{-2}	7.20×10^{-2}	8	200
Two-point	2.81×10^{-2}	7.28×10^{-3}	8	200
Two-point	1.49×10^{-2}	3.64×10^{-2}	10	200
Two-point	1.54×10^{-2}	4.03×10^{-2}	10	200

Two-point	1.90×10^{-2}	4.59×10^{-1}	12	200
Two-point	1.39×10^{-2}	2.97×10^{-1}	12	200
Two-point	2.19×10^{-2}	5.74×10^{-1}	12	200
Two-point	1.44×10^{-2}	2.98×10^{-1}	12	200
Two-point	2.24×10^{-2}	5.79×10^{-1}	12	200
Two-point	1.43×10^{-2}	2.82×10^{-1}	12	200

Table A.10. The wires here were coated with alumina.

Measurement Type	**Resistivity (untreated, Ωm)**	**Resistivity (annealed, Ωm)**	**Temperature (°C)**	**Time (min)**
Four-point	1.64×10^{-2}	1.78×10^{-3}	200	4
Four-point	3.51×10^{-2}	1.44×10^{-3}	200	4
Four-point	3.72×10^{-2}	3.11×10^{-3}	200	4
Four-point	6.44×10^{-3}	2.53×10^{-4}	400	4
Four-point	8.20×10^{-3}	5.96×10^{-6}	400	4
Four-point	1.11×10^{-2}	1.32×10^{-6}	400	6
Four-point	6.51×10^{-3}	2.06×10^{-6}	400	6
Four-point	5.83×10^{-2}	4.41×10^{-2}	200	6
Four-point	5.53×10^{-3}	1.20×10^{-2}	200	6

Appendix B

Definitions

Exposure

Subjecting a photoresist to a light, e-beam, or ion beam.

Develop

Once the photoresist is exposed, the resist is submersed in a chemical called a developer. The developer removes the parts of the resist that have been exposed.

Photoresist

A light sensitive material that coats a surface before patterning.

Lift-off

The process of removing the undamaged resist from a substrate after depositing a metal.

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