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Massively Parallel Indirect Dielectrophoresis Controlled Placement of Carbon Nanotubes

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MASSIVELY PARALLEL DIELECTROPHORESIS FOR CONTROLLED
PLACEMENT OF CARBON NANOTUBES

by

Hiram J. Conley

A thesis submitted to the faculty of

Brigham Young University

in partial fulfillment of the requirements for the degree of

Master of Science

Department of Physics and Astronomy

Brigham Young University

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BRIGHAM YOUNG UNIVERSITY

GRADUATE COMMITTEE APPROVAL

of a thesis submitted by

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This thesis has been read by each member of the following graduate committee and by majority vote has been found to be satisfactory.

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ABSTRACT

MASSIVELY PARALLEL DIELECTROPHORESIS FOR CONTROLLED PLACEMENT OF CARBON NANOTUBES

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Master of Science

Placement of single walled carbon nanotubes is demonstrated through massively parallel indirect dielectrophoresis (MPID). MPID is shown to be able to control the placement of carbon tubes as well as the number of tubes placed. Lumped element analysis for AC circuits is used to model MPID. This model allows for predictions of the number of tubes that will be captured in a trap. This model has been consistent with experimental data of numbers of nanotube placed in a junction. Carbon nanotubes placed with MPID are shown to be electrically active.

ACKNOWLEDGMENTS

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Chapter 1

Introduction

1.1 Carbon Nanotubes

Considerable excitement has surrounded carbon nanotubes since they were observed by transmission electron microscopy by Iijima in 1991[1]. Carbon nanotubes can be visualized as rolled up sheets of graphene that form a seamless cylinder. The carbon-carbon bonds in carbon nanotubes and graphene are sp^2 hybridized. This accounts for many of the phenomenal electrical and mechanical properties that have been reported in the literature. While carbon nanotubes can have many concentric walls, this thesis will focus on single wall carbon nanotubes (SWNT).

There are many theoretical ways to wrap a graphene sheet into a carbon nanotube. Carbon nanotubes are named according to this wrapping angle or chirality. The chirality is most commonly defined by the chiral index $C_h = na_1 + ma_2$ where a_1 and a_2 are the unit vectors of a graphene sheet as shown in figure 1.1. The chiral index determines the electrical properties and the diameter of the carbon nanotubes. If a carbon nanotube has a chiral index of $(n-m) \bmod(3) = \pm 1$ then it is semiconducting, all others are metallic.[2]

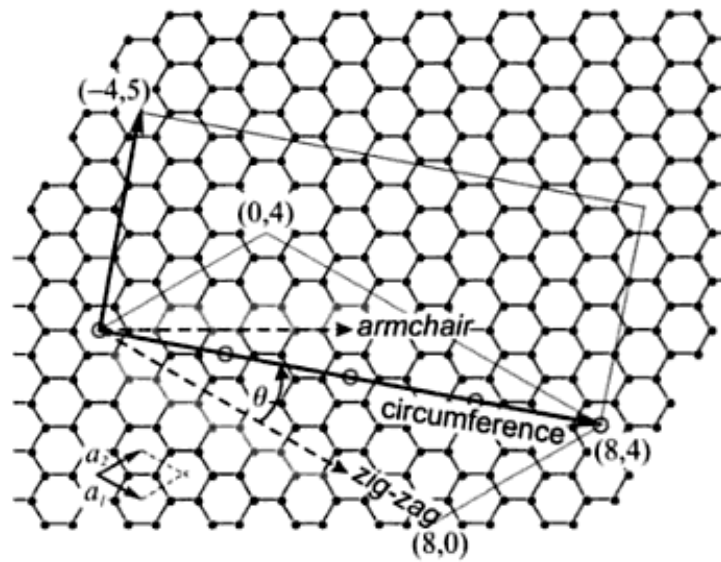


Figure 1.1: Graphene honeycomb lattice with unit vectors and chiral index. $C_h = na_1 + ma_2$ is the most common definition Chiral Index. a_1 and a_2 are the unit vectors of a graphene sheet. This figure is from the book by Reich et al[2].

1.2 Carbon Nanotube Electronics

Carbon nanotube's exceptional electronic properties make them interesting choices for future electronics. Carbon nanotubes have the highest electron mobility of any known semiconductor[3]. Due to this, semiconducting carbon nanotubes have impressive current carrying potential, with a current density up to 10^9 A cm⁻² as compared to high end silicon devices with a current density of 50^3 A cm⁻² [4]. These transistors have a transconductance and ON-current that are about a factor of 5 better than current state of the art silicon p-MOSFETs[5, 6]. Carbon nanotube transistors have a much lower capacitance and therefore lower switching energy [7]. Also carbon nanotube devices don't need to be made on expensive single crystalline silicon but can be made on plastics or other inexpensive and or flexible substrate [8].

Bachtold et al. built a carbon nanotube circuit by putting a single walled carbon nanotube on an aluminum wire and then putting gold wires onto the nanotube to create a circuit. In this fashion they created an "inverter, a logic NOR, a static random-access memory cell, and an ac ring oscillator"[9]. Most of the circuits made with carbon nanotubes were constructed by randomly putting carbon nanotubes on the surface. After finding the carbon nanotubes with an AFM, a circuit element was built over the carbon nanotube[9]. Others were built by randomly putting carbon nanotubes on top of parallel electrodes[10, 11]. Recently John Roger's group has used a quartz substrate to build massive arrays of horizontally aligned carbon nanotubes. They used these nanotube arrays to build FETs[8] and a functioning transistor radio.[12]. Jie Lu iused a clever growth method that incorporated methanol and ethanol to get arrays of aligned carbon nanotubes on quartz that are 98% semiconducting[13].

1.3 Challenges of Carbon Nanotube Electronics

In 2005 the International Technological Roadmap for Semiconductors reported, “The most difficult challenge for Emerging Research Materials is to deliver materials with controlled properties that will enable operation of emerging research devices in high density at the nanometer scale.” [14]

McEuen et al. states, “To date, there are no reliable, rapid, and reproducible approaches to creating complex arrays of nanotube devices. This manufacturing issue is by far the most significant impediment to using nanotubes in electronics applications. While there has been significant fanfare around circuits made with nanotubes, (see, e.g., the Breakthrough of the Year for 2001 in Science magazine), in reality the accomplishments to date are a far cry from anything that would impress a device engineer or circuit designer. However, there appear to be no fundamental barriers to the development of a technology.” [15]

One of the principle challenges that must be overcome before carbon nanotubes can be used in circuits is that there is no method for precise directed placement of carbon nanotubes.

1.4 Placement of Carbon Nanotubes

While this thesis will focus on dielectrophoretic placement of carbon nanotubes, it is important to realize that this technique is only one of several that attempt to control placement of carbon nanotubes. For a more complete overview of localization techniques of carbon nanotubes, including patterned growth methods, vertically grown nanotubes, spin coating, and dip coating, the author suggests the review article by Yan et al[16].

1.4.1 Dielectrophoresis

Dielectrophoresis was first discovered in 1950 by Herbert Pohl[17]. Dielectrophoresis is the force on a dielectric in an inhomogeneous electric field. The etymology of the word stems from dielectric, a broad classification of materials, and phoresis, the Greek word for force[18]. A dipole is induced in the dielectric when it is placed in an electric field. If the electric field is homogeneous the dipole experiences no net force, besides torque, and the particle does not move. Often dielectrophoresis is done in an AC field. This causes electrophoresis (the migration of charged particles in a homogenous electric field) to be limited.

Dielectrophoresis was first used to remove carbon black from various polymers[17]. In order to achieve the affect Pohl was required to use very large voltages (10000 V across a 1 cm wide cell) which made this technique less attractive. Modern dielectrophoresis has used microfabrication techniques to form the electrodes, allowing for more reasonable voltages to be used. In this study, for example, voltages from 5V to 20V were used. This is especially important in AC dielectrophoresis, as AC fields with large voltages are challenging to create. Dielectrophoresis has been primarily used in the life sciences for purification and control of cells[19] but has also been used

for placement of DNA[20], carbon nanotubes[21, 20], and silicon nanowires[22].

1.4.2 Force Due to Dielectrophoresis

This section relies heavily on the work done by Thomas Jones in his book Electromechanics of Particles[18]. The derivation is useful in order to understand dielectrophoresis and the experimental results in this study.

First we note the force a dipole will experience in an inhomogeneous field. If we think of a dipole as having a positive and a negative charge spaced by a distance d the force on a dipole can be written as equation 1.1.

$$F = qE(\vec{r} + \vec{d}) - qE(\vec{r}) \quad (1.1)$$

In the case that d is small compared to the field variation we can do a Taylor series expansion to yield equation 1.2.

$$E(\vec{r} + \vec{d}) = E(\vec{r}) + \vec{d}\nabla E(\vec{r}) + \dots \quad (1.2)$$

Inserting the first two terms of this equation into equation 1.1 yields the dipole approximation, equation 1.3. In this equation p is the effective dipole moment such that $p = qd$.

$$F = p\nabla E \quad (1.3)$$

From here we have several ways of accounting for particles. The first way to approximate a particle as a dipole is to say that a particle has a dipole moment proportional to an applied electric field. The proportionality constant is called the polarizability of a particle. This allows us to write equation 1.4.

$$F = \frac{1}{2}\alpha\nabla E^2 \quad (1.4)$$

Another way to think of the particles is as dielectrics in a dielectric medium. In order to find the force in this system it is useful to note the electrical potential of a dipole in a dielectric medium ϵ_1 . This is expressed in equation 1.5.

$$\Phi_{dipole} = \frac{p \cos(\Theta)}{4\pi\epsilon_1 r^2} \quad (1.5)$$

Then by remembering that solutions to Laplace's equation are unique we just need to find the electrical potential of a given geometry to know the effective dipole moment. This dipole moment can be inserted into equation 1.3 to yield an equation for the force acting on a dielectric particle. To illustrate this idea one can calculate the force on a spherical dielectric particle in an electric field by first noting:

$$\Phi_{outside}(r, \theta) = -E_0 r \cos(\theta) + \frac{A \cos(\theta)}{r^2}, r > R \quad (1.6)$$

$$\Phi_{inside}(r, \theta) = B \cos(\theta) r, r < R \quad (1.7)$$

Then by applying the proper boundary conditions, namely that the electric potential and the normal component of the electrical field must both be continuous across the boundary, one may solve for A and B. Then noting that it is that the potential outside the sphere and the potential outside of a dipole are the same, it is trivial to find the effective dipole moment of a dielectric sphere. This yields the force equation 1.8

$$F = 4\pi\epsilon_1 R^3 \frac{\epsilon_2 - \epsilon_1}{\epsilon_2 + 2\epsilon_1} \nabla |E|^2 \quad (1.8)$$

1.4.3 Dielectrophoresis of Carbon Nanotubes

Much work has been done on using dielectrophoresis to place carbon nanotubes between electrodes to make FETs[23, 24, 25, 26]. It has been shown that there are many ways to improve dielectrophoresis of carbon nanotubes. A $1\text{ G}\Omega$ resistor, put in series with the circuit that does dielectrophoresis, allows one tube to be placed between the electrodes while a large mat of carbon nanotubes are placed between the electrodes without the resistor. Metal posts with a floating potential have been put between electrodes and have helped guide placement of the nanotubes[25]. It has also been shown that nanotubes are more apt to bind individually to electrodes with a floating potential while clumps of nanotubes will bind to the electrodes that are being directly driven[23]. Nanotubes have been aligned across many devices at once with yields of 90%, demonstrating the possible scalability of the technique[26]. Recently Close et al used dielectrophoresis to place metallic carbon nanotubes as interconnects for silicon CMOS transistors, but with low yield.[27].

1.5 Massively Parallel Indirect Dielectrophoresis

Massively Parallel Indirect Dielectrophoresis (MPID) was developed in order to find a high yield scheme for placement of carbon nanotubes. The basic idea stemmed from the desire to place tubes on many devices at once and to place a single tube on each device. This led me to the basic design with two driving pads encapsulating multiple pairs of floating pads as shown in figure 1.2. The region between the pair of floating pads is called the dielectrophoretic trap and this is where carbon nanotubes should be localized.

The traps work under the basic principle stated by Herbert Pohl in his 1951 paper on dielectrophoresis. He states that dielectrophoresis “will deposit weights of sol [or in our case carbon nanotubes] in direct proportion to the voltage applied in equal times of deposition”[17]. In the case of carbon nanotubes this implies that higher voltages across the trap region will localize more tubes in the trap region. In MPID a voltage is applied to the driving pads, see figure 1.2. The traps work through capacitive coupling between the driving pads and the floating pads. This causes a voltage difference across the trap region. Once a carbon nanotube is captured the floating pads are electrically connected, decreasing the voltage difference and causing fewer tubes to be localized in the trap region.

1.6 Summary

In summary, carbon nanotubes are a promising material for future electronics due to their superior electronic properties and small size. MPID is presented as a possible route to overcome the challenge of carbon nanotube placement.

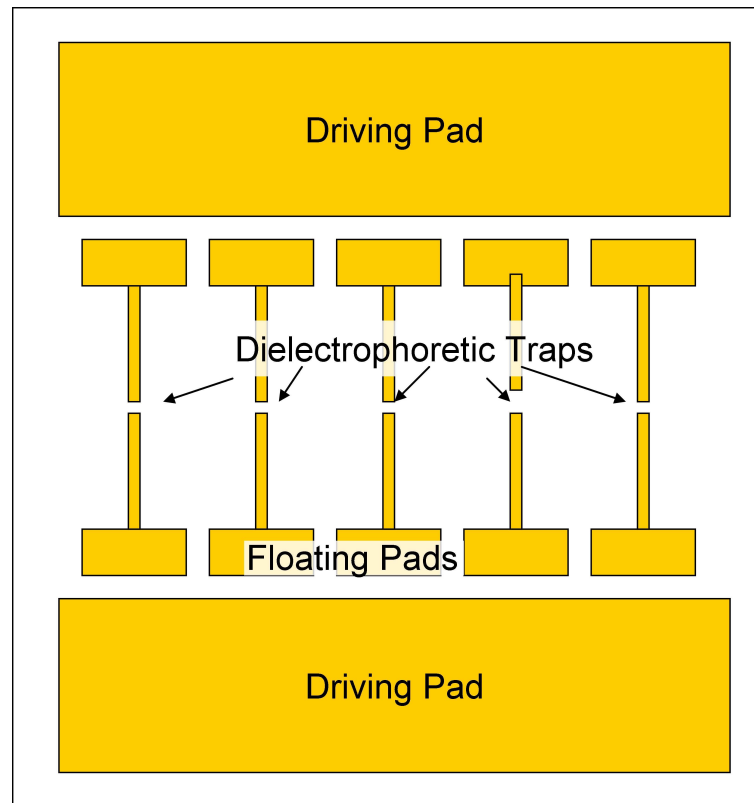


Figure 1.2: Basic schematic of a MPID device. An AC voltage is applied to the driving pads and carbon nanotubes are trapped in the trap region (the gap between the floating pads).

Chapter 2

Theoretical Modelling

In this chapter we explore a model of MPID. This model approximates the trapping of carbon nanotubes by MPID through lumped element analysis. Effects from various geometries such as silicon oxide thickness and floating pad size are presented.

2.1 The Simple Circuit Model for Carbon Nanotube Trapping in MPID

Referring back to equation 1.8 there is no clear explanation as to why only a given number of carbon nanotubes are captured in a trap. Here we present a closed form solution using lumped element analysis that provides an intuitive model to aid in design of MPID devices that can trap different numbers of carbon nanotubes.

The underlying assumption of this simple model relies on the idea that the trapping force on a carbon nanotube in a trap is proportional to the voltage difference across the trap region. Then by assuming that the gaps between the various pads and the substrate can be thought of as capacitors and the carbon nanotube as a resistor, one can find the voltage drop across the trap region using lumped element analysis as

shown in figure 2.1 and equation 2.1. In equation 2.1 the X referse to the impedance due to the capacitors. All subscripts can be identified with the componet on a MPID device through inspection of figure 2.1 and V is the voltage applied to the driving pads.

$$V_{trap} = \frac{X_{FS}X_{trap}R_{tube}}{X_{FS}X_{trap}R_{tube} + X_{trap}X_{DF}R_{tube} + 2X_{FS}X_{trap}X_{DF} + 2X_{FS}X_{DF}R_{tube}}V \quad (2.1)$$

The full result it is algebraic instead of a differential equation. One can easily plot the equation and explore the effect of modifying various parameters. For example it is apparent that V_{trap} has no dependance on the capacitive coupling between the driving pads and the substrate. The main parameters for the model is the capacitances of the various junctions. These are approximated by using the parallel plate capacitor model for the large pads. For the smaller pads or junctions where the parallel plate capacitor model is too crude the capacitances were approximated using finite elemental analysis (Comsol Multiphysics). Using this allows one to model the dependence of oxide thickness and pad size on the trapping power of the devices.

2.2 Trapping Power

One important aspect to model is the trapping power of a device. The trapping power is defined as the voltage difference across the trap region. In some sense the trapping power is arbitrary because one can increase the voltage as high as their equipment will allow. Yet at the same time increasing the voltage arbitrarily high is not often an option.

In order to model the effect of the oxide thickness on the trapping power one notes that $X_{FS} = -\frac{i}{\omega C_{FS}}$. In equation 2.1 X_{FS} is in the numerator so as X_{FS} approaches

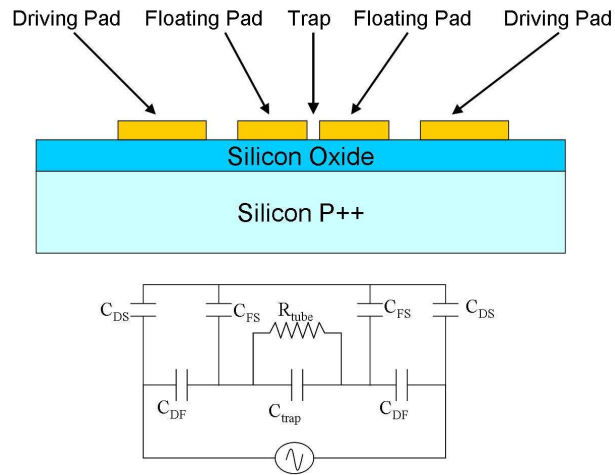


Figure 2.1: Cross section of MPID device with circuit representation of device. The trapping voltage was modeled using lumped element analysis. This is a schematic of a dielectrophoretic trap. C_{DS} is the capacitance between the driving pad and the substrate. C_{FS} is the capacitance between the floating pad and the substrate. C_{DF} is the capacitance between the driving pad and the floating pad. C_{trap} is the capacitance between the floating pads and R_{tube} is the resistance of a carbon nanotube in the trap.

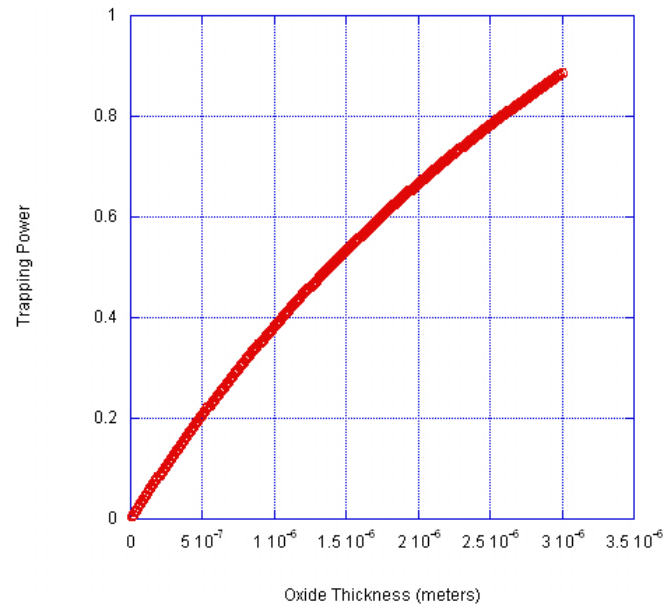


Figure 2.2: Oxide thickness (in meters) versus the trapping power of the trap. As the oxide gets thinner the trapping power decreases.

zero so does the trapping power. Using the parallel plate approximation to figure out the capacitance of these capacitors one can assume that the thinner the silicon oxide the smaller the trapping power. The parallel plate capacitor model allows access to model the effects of pad size and the distance between the capacitors, or the oxide thickness. In figure 2.2 the voltage across the trap region is plotted as a function of oxide thickness. The voltage across the trap region was much less with a thin oxide layer than with a thick oxide layer. This was done assuming that the floating pads were $25 \mu\text{m}^2$ and $10 \mu\text{m}$ from the driving pads. Figure 2.3 shows how the trapping power shuts off rapidly as the floating pad area becomes much larger.

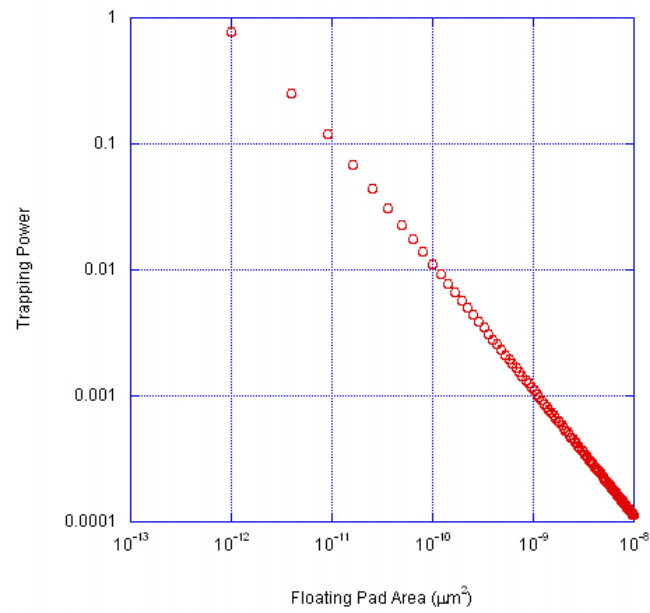


Figure 2.3: Floating pad area versus the trapping power. As the pads get larger much more voltage is required to trap the full number of tubes available to a trap.

2.3 Device Shut Off

Perhaps the most useful aspect of the modeling is the ability to predict a shut off resistance for the traps. The shut off resistance is defined as the inflection point when plotting the trapping power versus the resistance inside the trap region. This value is independent of the actual voltage placed across the driving pads and allows for a convenient way to track trends. A device that has a lower shut off resistance will trap more tubes.

Oxide thickness plays a role in the shut off resistance. Figure 2.4 shows a graph of devices with $100 \mu\text{m}^2$ pads with a 5μ gap between the driving and floating pads. As the oxide gets thicker the inflection point gets larger. One would assume that with the otherwise identical devices with different oxides, the one with the thicker oxide would trap less tubes.

Also the pad size affects the shut off resistance. As the pad size becomes larger the shut off value decreases, as shown in figure 2.5. In figure 2.5 the devices are with 100 nm of oxide and a $5 \mu\text{m}$ gap between the driving and floating pads.

It was also noticed that the gap between the floating and driving pads has an effect but that once the gap gets larger than a few microns a change in the gap does not affect the shut off resistance very much.

2.4 Limitations of Lumped Element Analysis for Modeling MPID

There are several limitations to lumped element analysis for predicting MPID effects. First our model extensively uses the parallel plate approximation in order to quickly calculate the capacitances for various configurations. This renders the model as weak

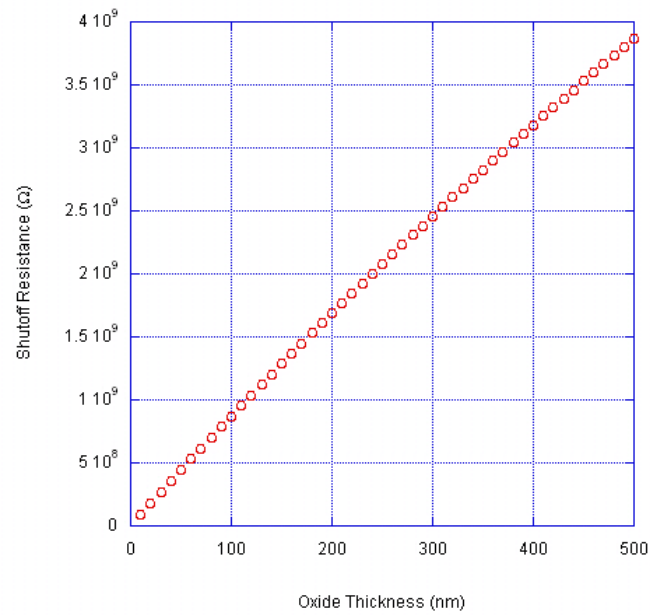


Figure 2.4: Oxide thickness (nm) versus shut off resistance. These traps have $100 \mu\text{m}^2$ floating pads that are $5 \mu\text{m}$ from the driving pad.

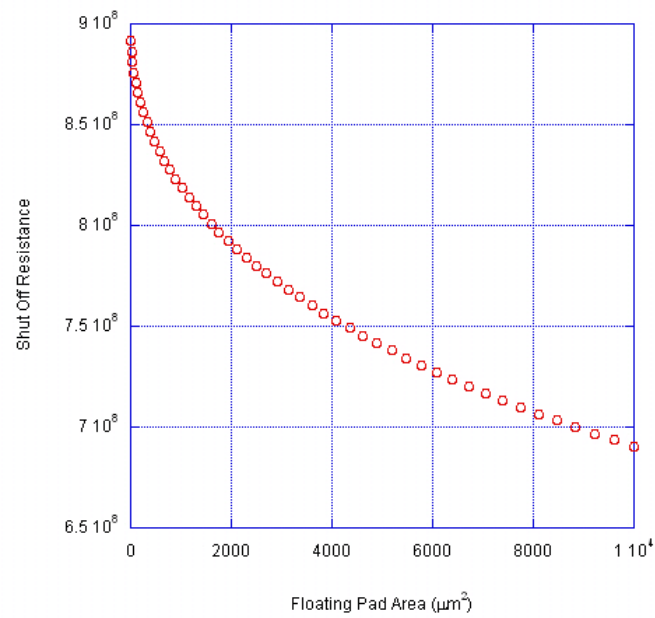


Figure 2.5: Floating pad area versus shut off resistance. It can be seen that as the floating pads become larger the shut off value decreases. This is modeled with 100 nm oxide and $5 \mu\text{m}$ gap between the floating and driving pads.

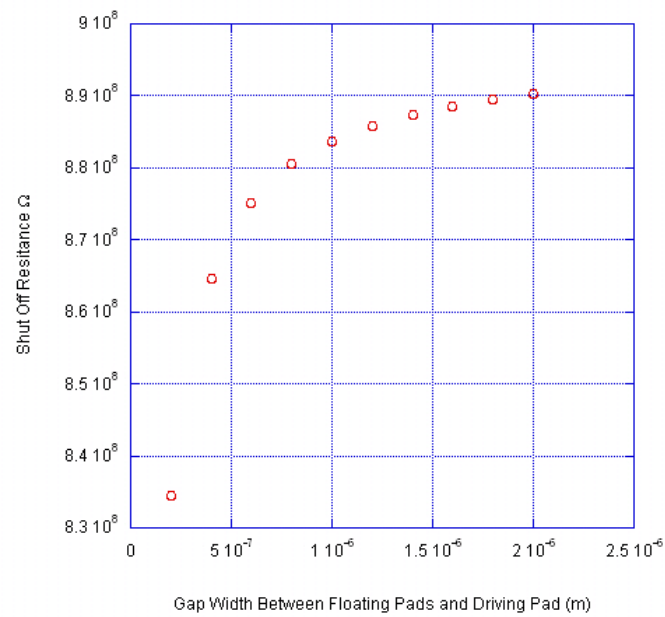


Figure 2.6: Gap between driving pad and floating pad versus shut off resistance. Once the distance becomes large enough the effect is small.

as the parallel plate approximation. This does not allow us to probe very small pad areas or very thick oxides. Also to find these capacitances is cumbersome with finite element analysis and can be very time consuming.

It should be noted that there are two distinct parts of the equation 1.8. There is the first part of the equation that is dependent of the geometry and material properties of the particle and the medium surrounding the particle. This is the particle part of the equation. The second part of the equation is the gradient of the electric field intensity. This is dependent on the geometry of the driving and floating pads and is the geometric part of the equation. The idea that the force is proportional to the voltage difference across the trap only accounts for the geometric part of dielectrophoresis.

Chapter 3

Methods

This chapter explains the fabrication techniques used to make MPID devices. The purification of the carbon nanotubes is also treated. Finally, dielectrophoretic placement of the carbon nanotubes onto the MPID devices is explained.

3.1 Fabrication of Devices

The first step in preparing MPID devices, see figure 3.1, is to growth thermal oxide onto silicon wafers. Oxide thicknesses are 20, 100, and 330 nm. The oxide is grown through a wet growth method at 1100° C. The wafers are broken into 1 cm² dies and ZEP520 (ZEON Corporation), an electron beam resist, is spun onto the oxide surfaces and then patterned with ebeam lithography. The dies are developed and then 5nm of chromium and then 25 nm of gold are evaporated onto the dies using an ebeam evaporator without breaking vacuum. The dies are soaked in acetone for 20 minutes and then sonicated in acetone for another 5 minutes. Then the dies are soaked in Shipley microposit remover 1165 at 70° C until the gold visibly lifts off of the surface, about 20 minutes.

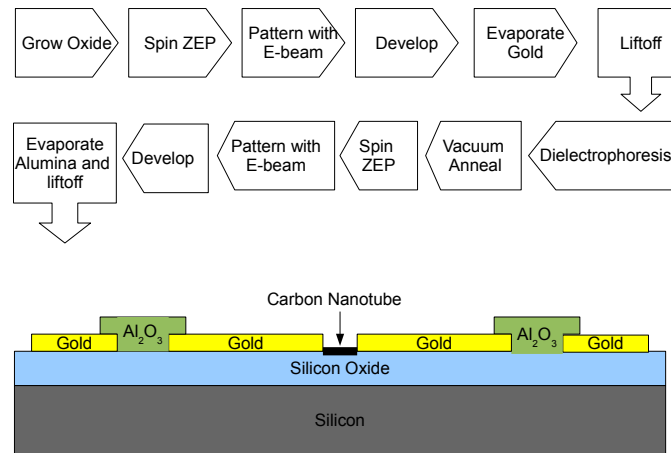


Figure 3.1: Process diagram and cross section of MPID devices.

For several of the experiments a layer of alumina is also deposited on the surface. A new layer of ZEP is spun on the gold patterned surface and after another ebeam lithography step, 30 nm of alumina is evaporated onto the surface in an ebeam evaporator. Liftoff is done as with the gold. An SEM image of an alumina device can be found in figure 3.2.

3.2 Purification of Carbon Nanotubes

To achieve an enriched sample of (7,6) carbon nanotubes, 2-5 mg of carbon nanotube soot (South West NanoTechnologies SG76) in 10 mL of HPLC grade water and 2 % weight sodium cholate are mixed. This suspension is sonicated with a horn sonicator for 2 hours with a 30% duty cycle. Care is taken to ensure the carbon nanotubes do not heat up by doing this in an ice bath. This results in a very black suspension that is then spun at 41000 rpm for 30 minutes to remove larger bundles of carbon

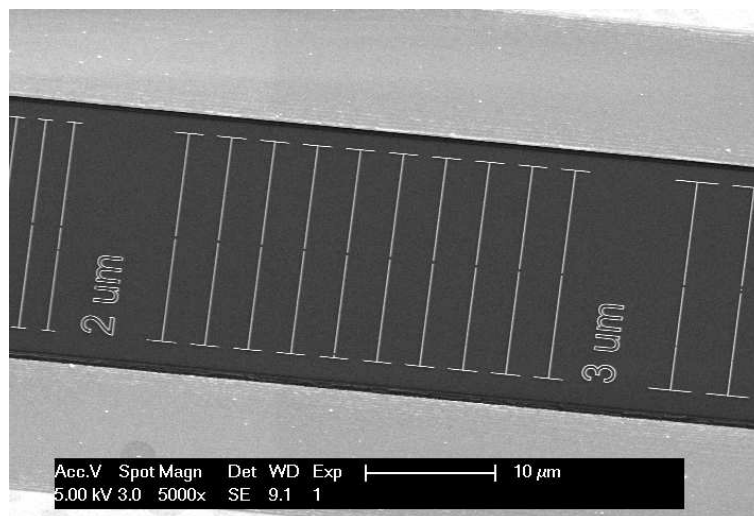


Figure 3.2: SEM image of dielectrophoretic traps. The devices are fabricated on silicon oxide and are made from Au with a Cr wetting layer.

nanotubes as well as the catalyst used to generate the carbon nanotubes. The top 80% of this suspension is harvested and then the tubes are concentrated by spinning at 41000 rpm on top of a layer of Optiprep Density Gradient Medium (SIGMA) with 2% weight sodium cholate for 7.5 hours. This leaves a tight black band of carbon nanotubes in the centrifugation tube. This band is harvested and put into a density gradient of Optiprep. After spinning this for 12 hours at 41000 rpm at 4° C distinct bands form with the top two bands being pink and green. These bands are harvested using a fractionation machine (BioComp Gradient Station) and used in MPID experiments. Bands are characterized using absorbance spectroscopy (Cary 5E UV-VIS-NIR Spectrophotometer).

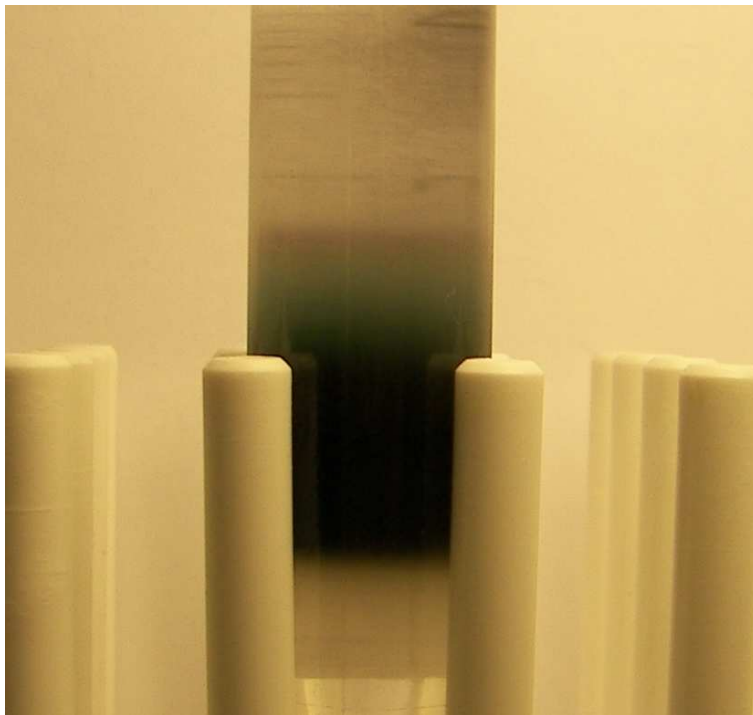


Figure 3.3: Carbon nanotube bands formed after centrifugation.

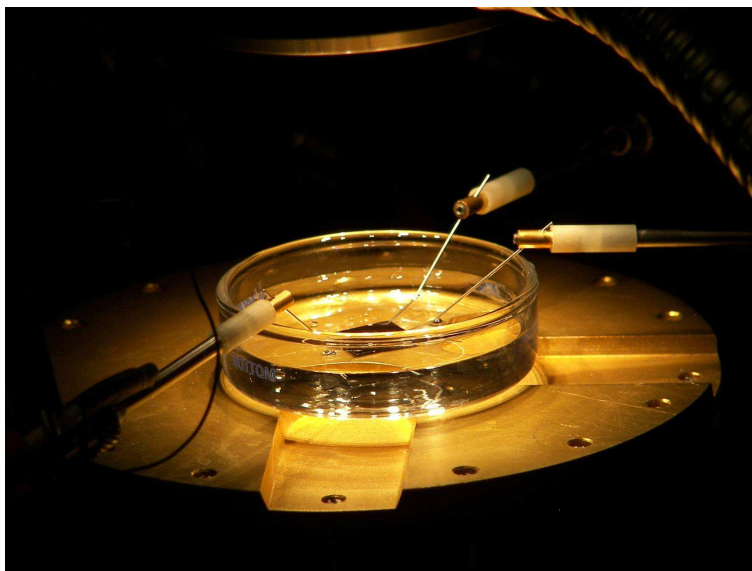


Figure 3.4: Photo of dielectrophoresis apparatus. Dielectrophoresis is performed by placing the die in a beaker of water and driving an electrical field on the driving pads through the micromanipulators shown.

3.3 Localization of Carbon nanotubes with MPID

To localize carbon nanotubes with MPID the patterned dies are placed in a beaker of DI water. Micromanipulators are used to place probes on the driving pads (see figure 3.4.) An AC signal is generated using a Wavetec or HP signal generator that is electrically connected to the micromanipulators. Careful control of the DC offset is necessary and for optimal performance DC offset was less than 10mV. For this study the voltages from 5 V to 20 V are used and the frequency, unless otherwise stated, is 50Khz. A drop of purified carbon nanotubes is placed in the water near the micromanipulators while the signal is generated. After waiting for about a minute the micromanipulators are removed and the die is rinsed with DI water to remove excess surfactant.

Trapped nanotubes are imaged using a Dimension V atomic force microscope

(Veeco) to confirm yield and quality of the placement of the tubes.

Electrical measurements are done using the same micromanipulators used for dielectrophoresis. Electrical measurements are done using MeaSureit, labview software made by Vera Sazonova. Some devices are annealed overnight in a vacuum oven at 100° C and their electrical properties are remeasured.

Chapter 4

Experimental Results

This chapter will first discuss spectroscopy of the carbon nanotube fractions. Then it will be shown that using MPID one can control the number of carbon nanotubes that can be placed in a trap. Also an overview of the electrical properties of carbon nanotubes localized with MPID is presented.

4.1 Spectroscopy of Carbon Nanotube Fractions

The carbon nanotubes from centrifugation are fractionated into .5 mm fractions. Each fraction was collected and analyzed using absorption spectroscopy. Each chirality of carbon nanotube produces a distinctive pair of peaks in absorption spectroscopy. This allows for identification of the chiralities in a fraction.[28]. Only semiconducting tubes are observable with absorbance spectroscopy.

Nanotube fractions were numbered from the top down, see figure 3.3, starting with fraction 1 and going to fraction 40. From figure 4.1 one can see the absorbance data from a few of the fractions. Fractions 10 and 25 were chosen because they represent the strongest peaks for (6,5) and (7,6) carbon nanotubes respectively. First it can be

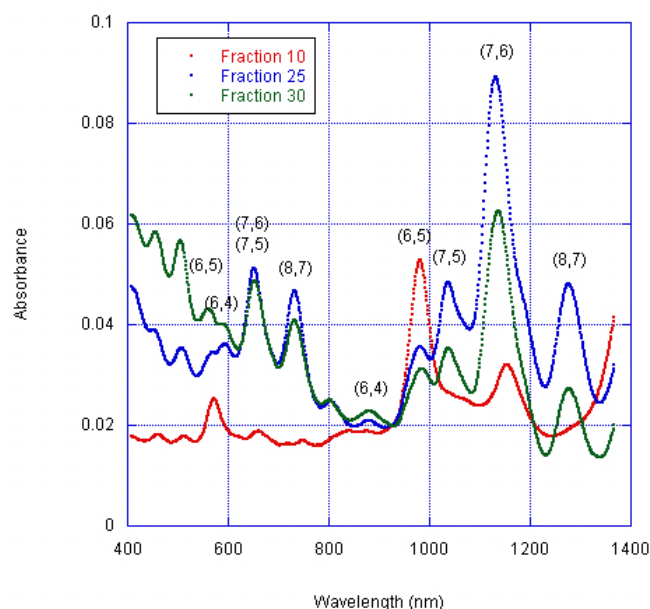


Figure 4.1: Absorption Measurement of 3 different fractions of purified carbon nanotubes. Fraction 10 is predominantly (6,5) chirality while the other fractions have a larger mix of carbon nanotubes.

noted that fraction 10 is predominantly (6,5) chirality. Fraction 25 has a much larger spread of tubes types but centered is on the (7,6) chirality. The main feature of note in fraction 30 is how the absorbance increases at lower wavelengths. This is caused by nanotube bundles and implies that there are bundles in the higher number fractions. It should also be noted that, in agreement with the theory of isopycnic centrifugation the more dense carbon nanotubes are found in the larger number fractions.

While many different fractions have been used with MPID, the focus has been on fractions that do not contain bundles. When making electrical measurements more care is taken as to which fraction is being used in order to correlate the electrical data

with the chirality of the carbon nanotubes.

4.2 Experimental Results of Carbon Nanotube Placement

Devices with different sized floating pads and oxide thickness trap different numbers of carbon nanotubes as shown in figure 4.2. Through balancing the capacitive coupling between the various capacitors one can capture a given number of tubes. For devices with $10000 \mu\text{m}^2$ floating pads and 100nm of oxide driven at $15 V_{pp}$, 30 devices were carefully examined and all 30 had large bundles of tubes that defied counting with the AFM or SEM. For devices with $25 \mu\text{m}^2$ floating pads with 100 nm thick oxide 20 devices were made under these conditions and all of them had 3 or 4 tubes in the trap region. For the devices with $25 \mu\text{m}^2$ floating pads with the 330 nm thick oxide 15 devices were observed, each with 2 to 3 tubes. For the T pad devices with a line width of 60 nm the yield was around 30% for single tube devices while the rest of the devices had tubes bridging between the floating pads and the driving pads, causing multiple tubes to be captured in the trap.

To verify that the devices shut off, devices with $25 \mu\text{m}^2$ floating pads had tubes deposited at $10 V_{pp}$, $11 V_{pp}$, $12 V_{pp}$ and $15 V_{pp}$. Of the ten devices deposited at $10 V_{pp}$ 8 of them were single tube devices, one of them had no tubes, and one electrode was damaged causing many tubes to deposit. For deposition of carbon nanotubes at $11 V_{pp}$ 5 of the traps captured single tubes, 4 captured 2 tubes, and 1 captured 3 tubes. The $12 V_{pp}$ deposition, 3 traps captured 1 tube, 6 captured 2 tubes and 1 captured 3 tubes. Of the 6 measured with a $15 V_{pp}$ deposition, 4 traps captured 2 tubes and 2 traps captured 3 tubes. This data can also be seen in figure 4.3.

Many pad sizes were examined. A series of devices had pads of various sizes. In

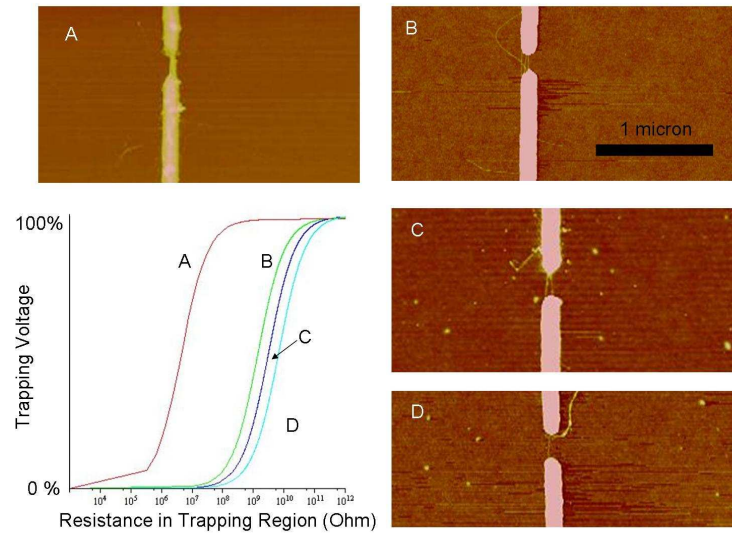


Figure 4.2: Trapping controlled number of carbon nanotubes based on shut off resistance. Here we tune device geometry to trap a given number of carbon nanotubes. The graph shows the modeled trapping voltage versus the resistance of the trap region. When a nanotube is added to the trap the resistance of the trapping region is reduced. A is $10000 \mu\text{m}^2$ floating pads with 100 nm oxide. B is $25 \mu\text{m}^2$ floating pads with 100 nm oxide. C is $25 \mu\text{m}^2$ with 330nm oxide. D is T shaped pads with a line width of 60nm and 330nm of oxide.

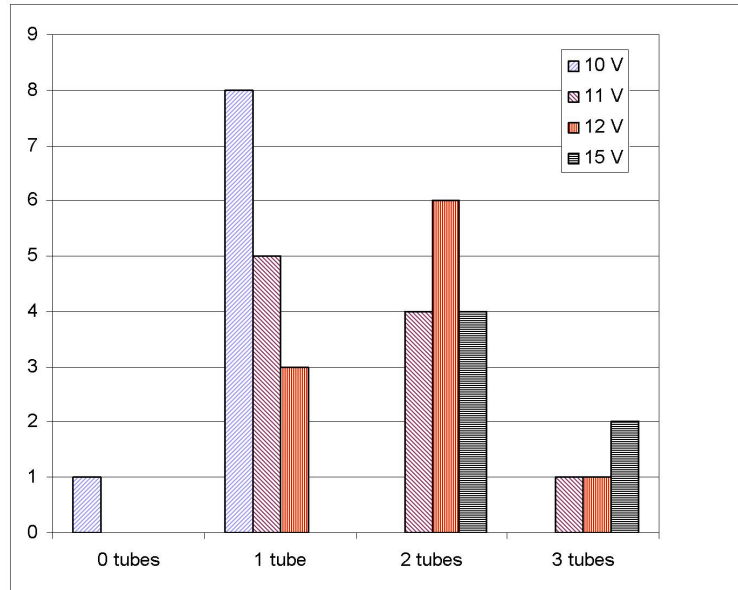


Figure 4.3: Histogram of number of tubes trapped in MPID traps at different voltages. All of these devices were with $25 \mu\text{m}^2$ floating pads on 330 nm of silicon oxide.

the same dielectrophoresis run the different pads trapped different numbers of tubes. The larger pads trapped more tubes while the smaller pads trapped less.

In the attempt to obtain high yield single tube devices a 30 nm layer of alumina was deposited between the floating pads and the driving pads. I also removed the T from the T pads and the floating pads only consisted of straight wires. The purpose of the alumina was to prevent carbon nanotubes from spanning the gap between the floating and driving pads. For 10 devices made this way all ten of them worked, each trapping 2-3 tubes (see figure 4.4).

A certain driving voltage is required to trap carbon nanotubes. This voltage is geometry dependent. For example, for $25 \mu\text{m}^2$ floating pads and 330 nm of oxide with a driving voltage $8 V_{pp}$ is needed to trap tubes, while traps with 60 nm wide floating pads and a layer of alumina between the floating and driving pads require $20 V_{pp}$ to trap tubes.

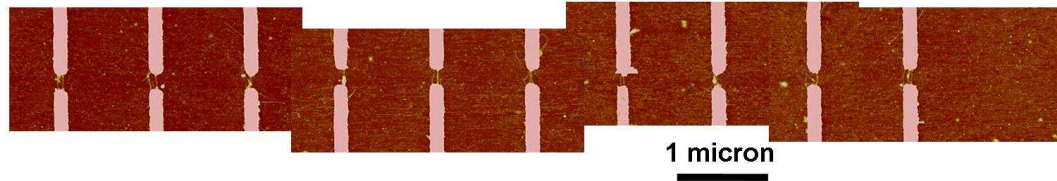


Figure 4.4: AFM images of devices with 2-3 tubes captured in each trap. This device has a 30nm thick layer of alumina between the floating pads and the driving pads. This changes the dielectric constant of the material between the floating and driving pads. Using the model to account for this 30nm thick alumina layer puts the curve near curve b in figure 4.2.

Various oxide thicknesses were studied. It was noted that no nanotubes were captured on devices made on thin thermal oxides of 20 nm. On oxides thicker than 100 nm dielectrophoretic traps capture carbon nanotubes.

It is possible to use less voltage than required to saturate a trap and still capture tubes. For example in our electrical studies $10000 \mu\text{m}^2$ pads were used. These devices naturally trap more tubes than can be counted with the AFM or SEM. We under drive the devices (i.e. use smaller voltages than required to saturate the trap, often near the limit where no tubes would be trapped) in order to capture less tubes. This technique, however, causes a drop in yield.

This under driven mode was used to study the frequency dependence of our devices. With a constant voltage of $8 V_{pp}$ across the driving pads with $10000 \mu\text{m}^2$ floating pads it was noted that at 2 KHz there was a large number of tubes coating the electrodes and that carbon nanotubes did not overly favor the trap. At 50 kHz nanotubes were constrained inside of the trap with 28 out of 30 devices trapping one or two nanotubes. At 200 kHz only 6 out of the 15 nanotube traps observed had

nanotubes.

If no voltage was applied to the driving pads no carbon nanotubes were trapped and were rarely observed on the surface. If a DC offset was present in the signal the floating pads and particularly the trapping region suffered extensive damage. Damaged traps either trapped no carbon nanotubes or a unpredictable number, which is attributed to changing and uncertain capacitances due to the random damage, device to device. If the driving signal was of poor quality, such as a driving signal produced by a Labview card, bubbles could be seen to form on the driving and floating pads and the pads would be lifted off of the surface. Tubes were not trapped in this case.

4.3 Electrical Properties of MPID Localized Carbon Nanotubes

Devices constructed using MPID are electrically active. All studies of electrical properties in this thesis are done on $10000 \mu\text{m}^2$ floating pads. This is due to limitations of the micromanipulator system used to make the electrical measurements.

Before annealing the carbon nanotube devices many of the devices had very little gate dependence. Devices had an average resistance of $100 \text{ k}\Omega$ with a devices ranging from 10 to $5000 \text{ k}\Omega$. After annealing the devices overnight in a vacuum oven at 100° C the electrical properties were very different. For a large number of devices the resistance of the tubes increased by an order of magnitude but the on/off ratio became much better, as can be seen in figure 4.5. While not every device became a perfect bundle of semiconducting tubes they all had the semiconducting behavior strongly enhanced. By counting the number of tubes in the devices with AFM and assuming that a device with a nanoamp of leakage current at 1 V_{SD} has one metallic

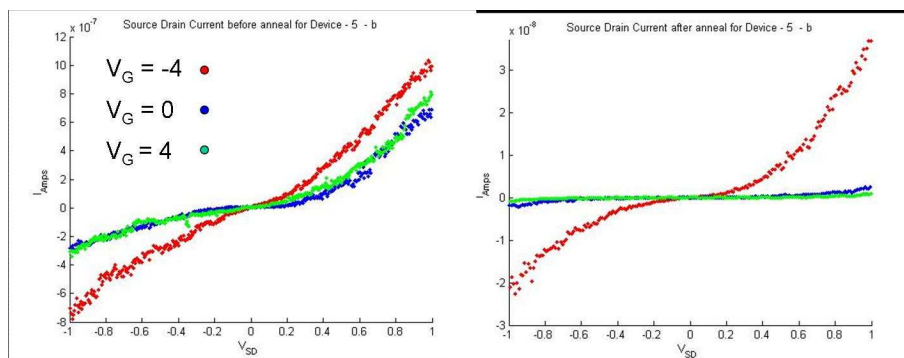


Figure 4.5: Effect on the electrical properties from annealing in vacuum at 100°C overnight. The resistance of the devices increases substantially but the devices are much more sensitive to a gate voltage.

tube the purity of fraction 25 (the fraction with the strongest (7,6) peak by absorption spectroscopy) I can state that fraction 25 contains about 95% semiconducting carbon nanotubes.

4.4 Summary

Nanotubes in solution can be enriched with various chiralities of carbon nanotubes. These nanotubes can be placed in large arrays with MPID. By tuning the pad size, oxide thickness, and the gap between the floating and driving pads the number of tubes localized in a trap can be controlled. Finally the carbon nanotubes show promising electrical properties.

Chapter 5

Discussion and Conclusions

This chapter shows that the simple model for MPID is in agreement with the experimental data. Various observed effects are noted and possible explanations offered. Limitations of MPID are discussed as are future experiments.

5.1 Model Accurately Predicts Experimentally Observed Trends.

There were several verifications of the capacitor model. First, carbon nanotubes are not trapped on devices made on 20 nm oxides. 100 and 330 nm thick oxides captured carbon nanotubes. Modeling of the trapping power versus the oxide thickness as done in figure 2.2 shows that the trapping power become much smaller as the oxide becomes thinner. I claim that as the oxide becomes very thin the trapping power is insufficient to trap carbon nanotubes.

Figure 4.2 shows a series of devices that trap different numbers of carbon nanotubes. The graph shown in the figure plots the trapping voltage versus the resistance inside the trap. By adding carbon nanotubes to the trap region the resistance of the

trap region decreases. Once a trap reaches a certain resistance the voltage decreases dramatically. This shows that the traps can be turned off by an impedance change in the circuit and is another confirmation of the simple circuit model for dielectrophoretic trapping.

In the 25um² floating pad study shows a nice example of trap shut off that happens when carbon nanotubes are trapped. Increasing the driving voltage does not trap more tubes. This follows the shut off shown in section 2.3.

Alumina was patterned between the floating pads and the driving pads. This is to prevent tubes from localizing between the floating and driving pads. Assuming the alumina would only prevent tubes from spanning the floating pad to the driving pads one would assume that these would be single tube devices, but they turned out to be 2-3 tube devices. The much lower dielectric constant of the alumina as compared to water lowers the capacitive coupling, shifting the shut off resistance, causing this effect.

5.2 Frequency Dependence of MPID

The high frequency cut off described in section 4.2 can be attributed to the observation that semiconducting carbon nanotubes will experience a negative dielectric force at sufficiently high frequencies[20]. As this cut off is dependent on the diameter of the carbon nanotubes it is expected that carbon nanotubes of different chiralities than the ones used in this study will have a different cut off frequency. The low frequency cut off is possibly due to electrophoresis dominating over dielectrophoresis at low frequencies. An interesting example of this can be seen with work on dielectrophoretic trapping of DNA origami[29].

5.3 Increasing Process Latitude

Harkening back to Pohls 1951 paper he states that dielectrophoresis “will deposit weights of sol in direct proportion to the voltage applied in equal times of deposition” [17]. The higher the voltage the more tubes will be deposited in a trap with dielectrophoresis. This was shown with DNA by Tuukkanen et al[30] were at one voltage they were able to trap one strand of DNA but by increasing the voltage they could trap more strands of DNA.

Attempting to make devices this way is tricky because a small change in the voltage will trap a different number of tubes. I spent several month attempting to localize carbon nanotubes this way and small changes in voltages had large effects on the number of carbon nanotubes captured. MPID allows one to design the number of tubes that will be localized in a trap primarily from the geometry. This increases the process latitude allowing for a broader range of voltages that will capture the same number of nanotube in each trap.

5.4 Saturation versus Under Driving Devices

In this study I note three voltage regimes. First when the voltage is too low no tubes are trapped. Second, called the saturation regime, when the voltage is sufficiently high that a small change does not have an effect on the number of tubes trapped. Then the final voltage regime, named the underdriven regime, between saturated regime and the regime were tubes are not trapped. In this regime less tubes are trapped then in the saturated case and some devices may not capture any tubes.

These three regimes can be explained by looking at figure 5.1. This figure shows three different driving voltages on the same device. The dashed line represents the minimum voltage required to trap a carbon nanotube. When doing MPID in the

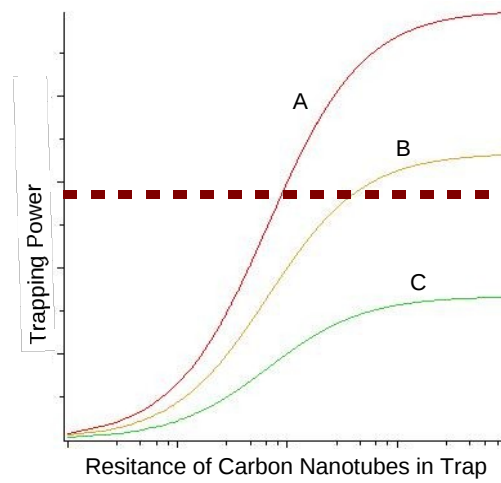


Figure 5.1: Three Driving Voltages. Lines A, B, and C represent three different driving voltages on the same device. The dashed line represents the minimum voltage required to trap a carbon nanotube. A represents the saturated regime, B represents the underdriven regime, and C shows the regime where no tubes will be trapped.

saturated regime the voltage is much greater than required to trap tubes up and until enough tubes are trapped that the voltage drops below the dashed line and the trap shuts off. This is the regime for a majority of experiments in this thesis. In this regime yields are over 99%. Several experiments in the underdriven regime are explained in the end of section 4.2. In this regime yield drops off. Single tube devices were also trapped in this regime. Looking at figure 5.1 one can see why the underdriven regime is less reproducible and why the yields are lower. One is near the minimum voltage required to trap a carbon nanotube and any defects in geometry could cause the voltage of a particular trap to be below the required to trap a carbon nanotube. Also if the voltage is a little too high a device will trap more than one carbon nanotube because the resistance required to shut off the device shifts over.

5.5 Annealing Devices

There was a dramatic effect on the electrical properties of MPID devices from annealing at 100° C overnight. The resistance and the on off ratio both increased. The temperature and the vacuum should in no way damage the carbon nanotubes and we have no reason to believe that this process could transform metallic carbon nanotubes to semiconducting carbon nanotubes. Also there is no evidence to suggest that selective destruction of metallic carbon nanotubes occurs in these conditions. So the change in the electrical properties must be attributed to another effect.

A possible explanation is that the carbon nanotubes in this study were wrapped with surfactant. The surfactant is charged and may cause both gating and screen the tube from the effect of gating. The vacuum anneal drives off the surfactant and leave use with normal carbon nanotubes.

5.6 Limitations of MPID and Future Studies

The main limitation in applying MPID to carbon nanotube electronics is that there is no perfect source of single chirality or even single electronic type carbon nanotubes. While density gradient centrifugation appears to be a possible route our research group has not been able to achieve purities required for large scale manufacture of devices.

Another limitation was that there is a distribution in the number of tubes trapped in each device. Instead of trapping precisely 4 tubes in a trap, there is a distribution of devices with 3 tubes and 4 tubes. If the tolerance for manufacture is exceedingly tight, MPID may not be a good solution.

On the other hand improving the distribution is an interesting area of future research. Engineering devices such that the shut off is much sharper should narrow the distribution in the number of tubes trapped in each device.

Future investigations of MPID could include using MPID to construct devices such a circuits or sensors. Also we have shown in this study that yields are greater than 99% for multitube devices. While this is a good yield in order to use MPID for microelectronics the yields need to be much higher. Studies to find the true yield would demonstrate if MPID is practical for microelectronics.

A systematic study of other nanoparticles such as quantum dots and the plethora of nanotubes and nanowires being currently produced would be interesting with MPID. MPID would allow for a simple way to localize these materials to study their individual properties. Also it would demonstrate if MPID is a more general technique or is limited to carbon nantubes.

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