The Physics of Low-Capacitance JFETs

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The Physics of Low-Capacitance JFETs

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Abstract

An important problem in the development of x-ray detectors is minimizing the input capacitance of the preamplifiers. The maximum signal is transmitted to the FET in a charge-sensitive preamplifier when the capacitance of the detector and the FET are equal. This thesis targets the designing of a minimized small gate capacitance JFET, and on a consideration of manufacturing and testing against theory by fabricating some device structures.

In this thesis, I show that gate length *l* is one of the most important geometrical parameters for creating a low capacitance and high gain device. Another important consideration concerns the etching technique. Even with alignment within 0.5μm, if etching technique does not involve a careful consideration of chemical concentration and timing relative to thickness of the oxide, the device cannot be successfully fabricated. Third, the shallow gate necessary for a successful low-capacitance device can only be achieved by using low energy ion implantation.

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This thesis by Pavel L. Brovkin is accepted in its present form by the Department of Physics and Astronomy of Brigham Young University as satisfying the thesis requirement for the degree of Master of Science.

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1. Introduction and background

Brief history of JFETs

Surprisingly, the invention of the field-effect transistor (FET) actually precedes by many years the classical works of Bardeen, Brattain, Pearson, and Shockley in the late 1940's. Their work led to the invention of the point-contact and bipolar transistor). In 1925 and 1926 J.E. Lilienfeld filed Canadian and U.S. patent applications entitled "Method and Apparatus for Controlling Electric Currents,"[1] in which he disclosed a semiconductor device using a gate electrode. A further patent application in 1935 by O. Heil [2], who was apparently unaware of Lilienfeld's work, also describes a thin film field-effect device with either one or two gates to control the current.

Serious work on these devices was not continued until the late 1940's, when studies undertaken at the Bell Telephone Laboratories were initially directed towards designing a surface field-effect device. Results reported by Shockley and Pearson in 1948 were discouraging. In their experiment they used a thin film of germanium separated from a metal field electrode by a thin film of mica. The change in conductance of germanium film as a function of the gate potential was measured by two electrodes attached to the sample. It was found that the degree of modulation obtained was considerably less than was predicted by assuming that all the charge induced in the germanium was free to move. It was found that only 10% of the induced charge was effective in changing of the conductance; the remaining 90% was trapped in surface states which were rendered immobile[3].

In 1952 Shockley reported a new device which was radically different from the bipolar transistor. In the new device, the majority carrier current was modulated by altering the thickness of a conducting channel through the narrowing or widening *p-n* junction depletion layer. Since the conducting channel appears well away from the semiconductor surface, the effects of the surface traps have a negligible effect on the device's operation, thus bypassing the problems of the earlier field-effect devices[4].

Further research of FETs in the late 1960's ended with well-designed devices high in gain and with low capacitance in the depletion region. Since then, research and production were aimed primarily at metal-oxide semiconductor field-effect transistor (MOSFET) technology, while junction field-effect transistors (JFETs) were neglected for many years because of their high-frequency limitations. However, the fact that JFETs have lower noise than MOSFETs or bipolar junction transistors (BJTs) has yielded applications for various types of sensors. One of these applications is the first amplification stage for a silicon-based x-ray detector. Since interest in low-noise and low-capacitance JFETs has been expressed only in the last few years, the designs for high performance JFETs for these applications have not yet matured.

The purpose of this thesis is to explore the design and fabrication of JFETs for these applications and identify some of the key problems in fabrication of low capacitance devices.

2. Statement of problem and objectives

Summary of Objectives

I have chosen to address the physics aspect of this problem involving capacitance, avoiding issues which are of circuit-dependent nature, such as load resistance. I will:

1. Present JFET theory and explain why the g_m/C_g ratio (tranconductance over gate capacitance) needs to be high and briefly consider the signal/noise ratio.
2. Discuss the simulation process for a low capacitance JFET. This simulation is done in order to understand what processes could be used to prepare such a structure, and how to select among alternate processes to produce the highest g_m/C_g.
3. Compare the simulated structure and design with that of existing low-noise, low-capacitance JFETs, used in the first stage of an x-ray detector amplifier.
4. Present my attempts to prepare a JFET, which identify some of the difficulties that are encountered in fabricating low-noise, low-capacitance JFETs. Here, I also address the question of the feasibility of creating a state-of-the-art device in a clean room meant for university instruction.

Statement of Problem

An important problem in the development of x-ray detectors is minimizing the input capacitance. The maximum signal is transmitted to the FET in a charge-sensitive preamplifier when the capacitance of the detector and the FET are equal. The influence of other

considerations, such as stray capacitance and the FET voltage noise have caused some designers to bypass this rule and demand the smallest possible FET capacitance regardless of the detector capacitance. Charge sensitive preamps are designed so that the gain of the input FET is high enough that noise from succeeding stages of the preamp is insignificant[5]. However, the above is not true for ultra-high resolution systems. Thus such systems could benefit from higher-gain FETs. In other words, in order to develop high-resolution X-ray detectors it is necessary to reduce the noise and the capacitance of the JFET detectors. One of the important parameters of the JFET is transconductance:

$$g_m = \frac{\partial I_d}{\partial V_{ds}} \qquad (1),$$

where I_d and V_{ds} are channel current and drain-source voltage, respectively. This parameter is proportional to the ratio of the gate width Z over the channel length l. Sometimes, in electrical engineering, this parameter is associated with gain, where maximum gain for the JFET is

$$A_v = g_m R_{ds} \qquad (2),$$

and where R_{ds} is the resistance between drain and source.

At the same time, gate capacitance, C_g, will be proportional to the product of Z and l. Thus, as gain is increase and capacitance is reduced, we also should increase the geometry-dependent ratio:

$$F = g_m / C_g. \qquad (3),$$

which will be discussed later (see equation 20, p. 29)[6].

My research is going to focus on one of the problems discussed above, namely the designing of a minimized small gate capacitance JFET, and on a consideration of manufacturing and testing against theory by fabricating some device structures.

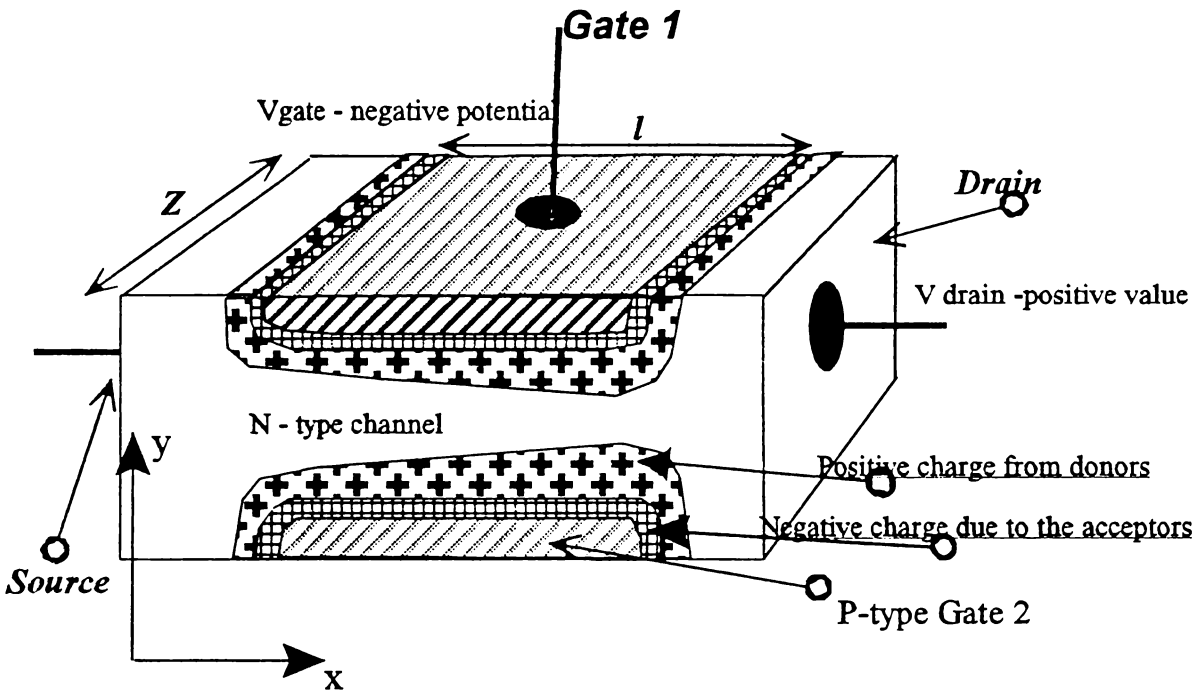


Figure 1. Depletion regions of Junction Field Effect Transitor.

3. The Theory

In this section, I will discuss the role of the ratio g_m/C_g and will consider noise in the next. I will demonstrate two main points; that transconductance (g_m) is dependent on a geometric parameter that is proportional to gate width over length (see equation 10), and that the capacitance is proportional to width multiplied by length (equation 19). First, let us consider the devices shown in Figures 1 and 2. This device, called the JFET, consists of an N-type

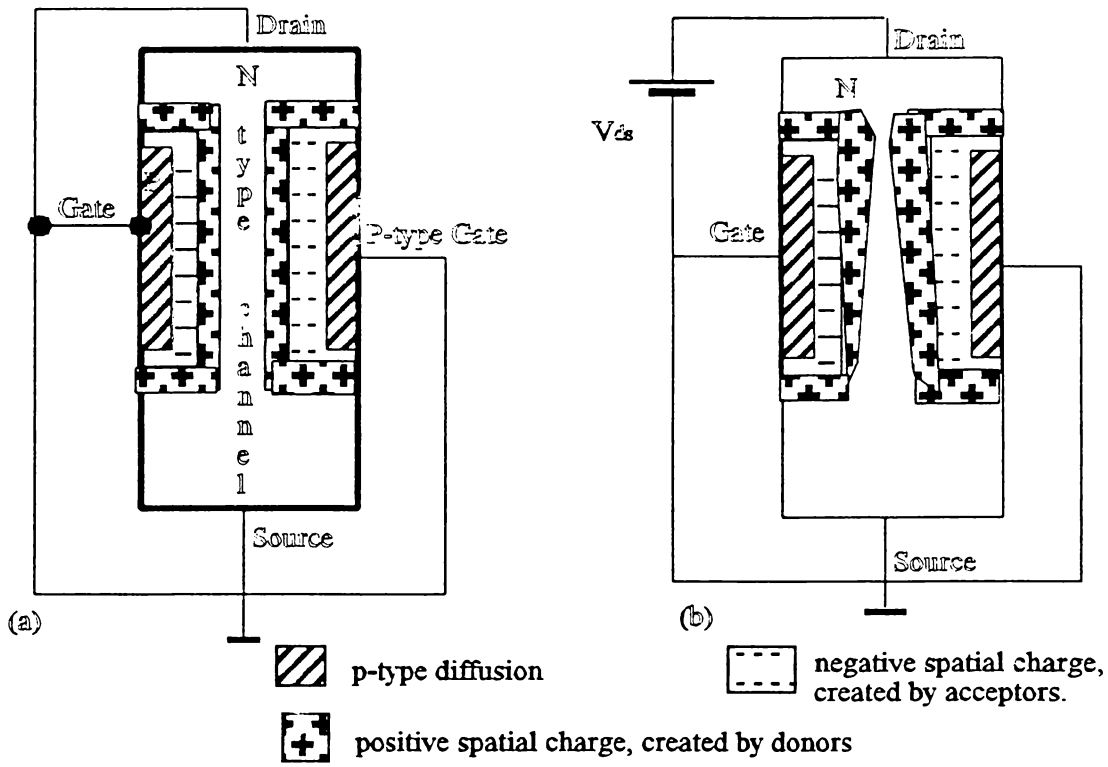


Figure 2: Schematic cross section diagram of the n-channel JFET under

a) Zero bias on all electrodes
b) Positive drain-source voltage and zero gate voltage.

channel sandwiched between P-type gates. The channel is formed by source and drain electrodes. The source acts as an origin of the carriers, and the drain as a sink. If there is no applied voltage on the electrodes, the space charges still exist on the metallurgical junction: gate-source or gate-drain, due to the parameter called the "built-in junction potential" -- V_{bi}. If we apply a potential on one of the electrodes, the charge distribution will be altered. In Figure 2, case (b), is shown the effect of increasing the drain-source voltage V_{ds}. As a result, the flow of current in the channel will increase (the drain will be more positive). This will cause the space charge to be greatest nearer the drain. A further increase in drain voltage results in an increase in reverse bias on the gate-channel junction. This will lead to an increase in spatial charge in the junction. Due to this spatial charge change, the channel resistance will increase. Eventually, we will reach a pinch-off condition at the drain, also called saturation. The gate-drain voltage at which this occurs is called the pinch-off voltage V_{po}. Note that V_{po} is a negative value. This parameter, V_{po}, is a very important one for the characterization of the JFET. The drain current does not necessarily have to be at zero when the pinch-off voltage occurs. It does, however, remain constant after this voltage, and forms what is called the saturation region. The space charge will form the gate-drain and gate-source capacitance. Under normal operating conditions, the gate bias is maintained such that a reverse bias (V_{gs} gate-source bias) exists along the length of the gate-channel and junction. That will form –compared with the source-drain -- an extremely small gate current. Typically, the input resistance of the gate is very large -- $1x10^9\ \Omega$ for a silicon device. If the gate voltage increases (towards the positive potential), the channel

widens, and the drain current increases. The typical drain-source resistance for a small silicon device in saturation is approximately 30kΩ.

The formulaic definition of transconductance is:

$$g_m = \partial I_d / \partial V_{gs} \qquad (4).$$

For the typical device, the transconductance g_m ~0.1m℧. By increasing the ratio of width over length *(Z/l)* the transconductance can be increased. The largest typical value is approximately 0.1℧. The electrical engineering characterization equation for a JFET for drain current in saturation, as given by Middlebrook[7], is

$$I_d = I_{dO} (1 - V_{gs}/V_{po})^{n.} \qquad (5)$$

where I_{dO} is the drain current when $V_{gs} = 0$, V_{po} is the pinch-off voltage when the channel is pinched off at the drain region by the gate reverse bias, and n is a constant, usually between 1.5 and 2.5. In this case, the equation for maximum transconductance could be derived from the previous equation, as the following:

$$g_m = \frac{nI_{ds}}{V_{gs} - V_{po}} \qquad (6)$$

where I_{ds} is the saturated value of the drain current. It can be found that g_m is at maximum value when $V_{gs} = 0$. Let us call this maximum transconductance value g_{mo}. Then:

$$g_{mo} = \frac{-n}{I_{dO}} \quad V_{po} \qquad (7)$$

We can see the ratio is

$$\frac{g_{mo}}{I_{dO\ (max)}} \approx 2.0 \text{ Volts}^{-1} \qquad (8).$$

This ratio can be achieved by simply substituting n=2.0 and V_{po} = -1 Volt.

The exact circuit model of the channel and the gate regions can be illustrated by Figure 3a.

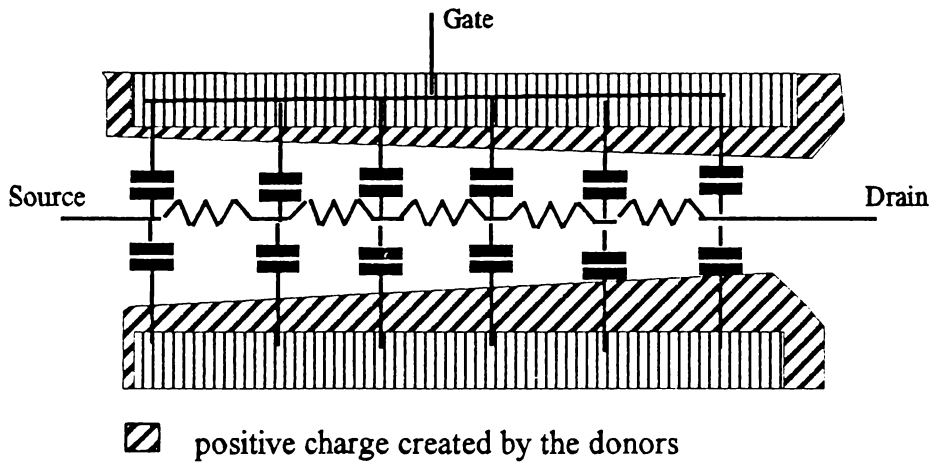


Figure 3a: Distributed lumped circuit model of the channel region of the JFET.

This circuit has little practical use because of its complexity. It could be replaced by an approximate intrinsic circuit model, shown in Figure 3b.

In this circuit, V_{gs} represents the input voltage (potential of the gate). The elements C_{gd} and C_{gs} (gate-drain and gate-source capacitances) represent the total gate-channel capacitance, as R_{gs} and R_{ds} represent the effect of channel resistance. Usually C_{gd} becomes zero if we have saturation conditions. We could represent the rise time coefficient as

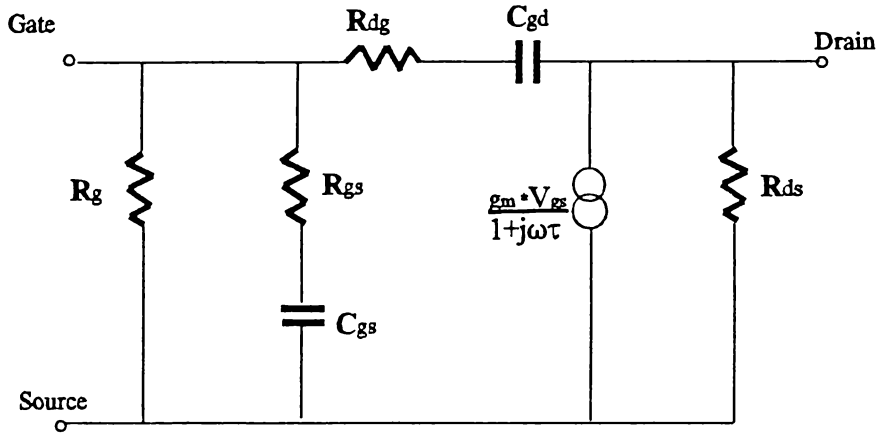


Figure 3b: Approximate high frequency circuit model of JFET

$$\tau \approx \gamma C_{gs} R_{ds}. \quad \gamma \approx 2.0. \tag{9}$$

For the drain- source conductance we could derive the equation in term of parameters ***l*** and ***Z*** (which are length and width of the gate respectively) (see endnote seven),

$$g_m = \frac{2aZq\mu_n N_n}{l} \tag{10}$$

where a is half the channel thickness, and Z and l are shown in Figure 1 (channel width and channel length, respectively). N_n and μ_n are the dopant concentration in the channel and mobility of the carriers. This formula came from the integration of g(V) over the entire space charge region (see discussion and equation 13 below), and with the assumption that the saturation condition (pinch-off voltage) reached. This formula will be very useful later.

The Capacitance of a JFET

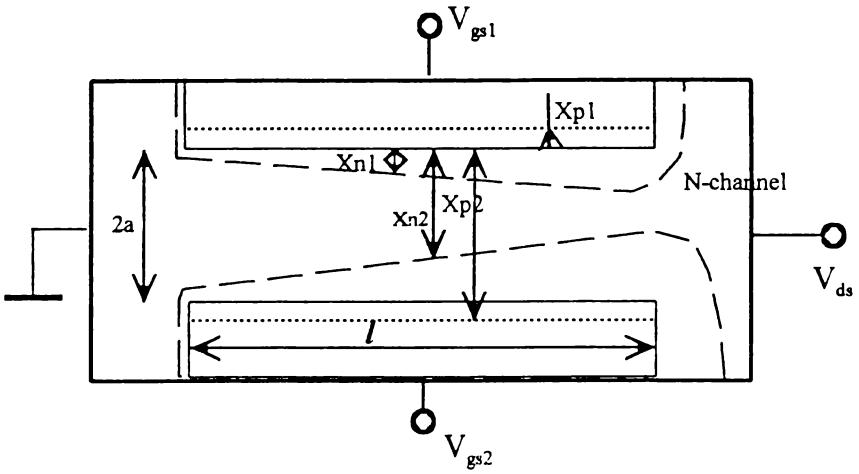


Figure 4a Approximate charge distribution in four-terminal JFET.

For the JFET shown in Figure 4a, the intrinsic channel charge can be expressed as:

$$Q_i = qZ\int_O^l (\int_0^{x_{n1}} (N(x)dx + \int_{x_{n2}}^{2a} N(x)dx)dy \tag{11}$$

where N(x) is the doping concentration and x_{n1} and x_{n2} are the locations of the two depletion edges. Using the expression for the electric field along the channel,

$$\frac{dy}{dV} = \frac{-l \cdot g(V)}{I_d} \tag{12}$$

we can substitute it into equation 11, where V is the gate-channel potential, and

$$g(V) = \frac{Z}{l}\int_{x_{n1}}^{x_{n2}} q\mu_n N(x)dx. \qquad (13)$$

This will give us equations 14 and 15:

$$Q_i = \frac{-Zlq}{I_d}\int_{V_{gs1}}^{V_{gs1}-V_{ds}} g(V)\left(\int_0^{x_{n1}} N(x)dx + \int_{x_{n2}}^{2a} N(x)dx\right)dV_1 \qquad (14)$$

$$Q_{i2} = Q_{i2}(V_{gs1}, V_{gs2}, V_{gs2} - V_{ds}) = \frac{-Zlq}{I_D}\int_{V_{gs2}}^{V_{gs2}-V_{ds}} g(V)\left(\int_0^{x_{n1}} N(x)dx + \int_{x_{n2}}^{2a} N(x)dx\right)dV_2$$

(15).

V_1 and V_2 are the gate-channel potentials at the y-axis (refer to Figure 1). The charge at the gate 1 (Q_{i1}) can be easily expressed with equation 15, simply by reversing the indices of notation as they appear in this formula so that where there is a one there should be a two and vice versa. From this, we can derive the capacitance of the gate:

$$C_{gs1} = \frac{-\partial Q_{i1}}{\partial V_{gs1}} \qquad C_{gd1} = \frac{\partial Q_{i1}}{\partial V_{ds}}$$
$$C_{gs2} = \frac{-\partial Q_{i2}}{\partial V_{gs2}} \qquad C_{gd2} = \frac{\partial Q_{i2}}{\partial V_{ds}}$$

(16).

Using these partial derivatives, we can arrive with the formula for channel-gate current:

$$I_s - I_d = C_{gs1}\frac{dV_{gs1}}{dt} + C_{gs2}\frac{dV_{gs2}}{dt} + C_{gd1}\frac{d(V_{gs1} - V_{ds})}{dt} + C_{gd2}\frac{d(V_{gs2} - V_{ds})}{dt} \qquad (17)$$

Using the symmetrical abrupt junction approximation, we will arrive at the following expressions

for the channel depletion charges:

$$Q_{i1} = \frac{-a^2 Z^2 N_n^2 q^2 \mu_n}{I_d} \int_{V_{gs1}}^{V_{gs1}-V_{ds}=V_{gd1}} \left\{ 2\left(\frac{V_1}{V_0}\right)^{1/2} - \frac{V_1}{V_0} - \left[\frac{V_1\left(V_{gs2} - V_{gs1}\right) + V_1^2}{V_0^2} \right]^{1/2} \right\} dV_1$$

$$Q_{i2} = \frac{-a^2 Z^2 N_n^2 q^2 \mu_n}{I_d} \int_{V_{gs1}}^{V_{gs2}-V_{ds}=V_{gd2}} \left\{ 2\left(\frac{V_2}{V_0}\right)^{1/2} - \frac{V_2}{V_0} - \left[\frac{V_2\left(V_{gs1} - V_{gs2}\right) + V_2^2}{V_0^2} \right]^{1/2} \right\} dV_2$$

(18)

(For those interested in the algebraic derivations of the previous formulas, please refer to Theory and Applications of Field-Effects Transistors, Richard S. Cobbold, Wiley-Interscience, NY: 1970).

In saturation conditions, the gate capacitance,

$$C_{gg} = \frac{\partial Q_{i2}}{\partial U_{gs1}} \qquad (19),$$

could be expressed as

$$C_{gg} = \frac{lZ\varepsilon_s}{x_{p2} - x_{p1}} \qquad (20).$$

Formula 20 is derived by integrating capacitance for the parallel plate capacitor (Figure 4b), which means that it is only valid for parallel plate approximations. I should mention that charge

neutrality requires that

$$\int_{xp1}^{xp2} qN(x)dx = 0 \qquad (21).$$

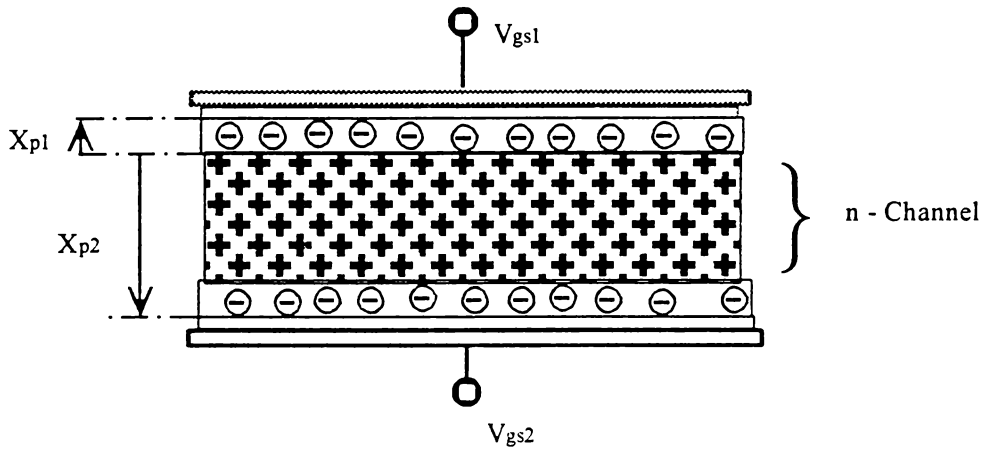


Figure 4b Charge distribution under parallel plate approximation.

From formula 20, we can see that the gate-capacitance will depend on the width of the gate *l*, channel length *Z*, and the depletion width (x_{p1} and x_{p2}). From this we may conclude that in order to decrease capacitance of the gate, we must narrow the gate and decrease the channel length. In order to increase the transconductance (g_m), we must increase the *Z/l* ratio. This will impose certain restrictions upon the technological design of the masks and upon the process description, that is, how to make the gate shallower. We could see that in order to create a JFET with low gate capacitance and not lose the transconductance, we should make the gate as narrow as possible.

4. Noise Consideration

The noise factor could be expressed as a dimensionless noise figure (F_N). High F_N marks

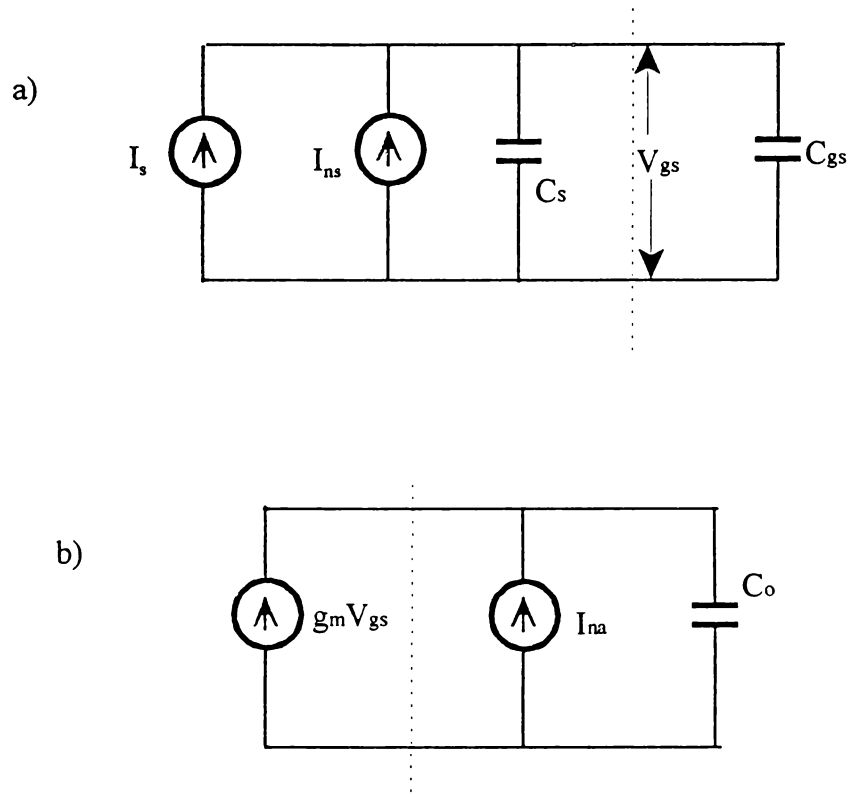


Figure 5 Diagram for JFET demonstrating noise considerations for a) input energies, b) output energies.

the lowest increase of noise for the JFET. Although this thesis targets mostly capacitance considerations, noise poses an interesting problem. It can be shown that the noise figure is also dependent upon the g_m/C_g ratio. This means that a low capacitance problem is related to designing a low noise JFET -- the goals are complementary. In fact, the noise figure can be expressed in a simple formula:

$$F_N = \frac{S_o / N_O}{S_{in} / N_{in}} \qquad (22),$$

where S_0 and S_{in} are the available energies of the signal, and N_{in} and N_0 are the available noise energies. From now on, in formula subscripts for any variables or constants, the abbreviation "o" means output, "in" means input. In figure 5, I_{na} is the output amplifier's current, and C_{gs} is gate-source capacitance, used later in this thesis as C_g.

The energy associated with any capacitor is expressed as the following:

$$Energy = \frac{1}{2}CV^2 = \frac{1}{2}C\frac{I^2\Delta t^2}{C^2} \qquad (23),$$

since $V = \frac{q}{C}$ and $q = I \cdot \Delta t$. V_{gs} can be expressed as:

$$V_{gs} = \frac{I_s \Delta t}{(C_s + C_{gs})} \qquad (24).$$

Noise energy for the amplifier is calculated in formula 25,

$$N_0 = \frac{1}{2}C_o V_{ds}^{\ 2} \qquad (25)$$

where V_{ds} is drain-source potential, and C_o is output capacitance (or drain capacitance). Then the ratio of energies is expressed as follows:

$$\frac{S_{in}}{N_{in}} = \frac{I_s^2 \Delta t^2 / 8C_s}{I_{ns}^2 \Delta t^2 / 8C_s} \qquad (26).$$

$$S_o = \frac{g_m^2 \Delta t^2}{8C_o}\left[\frac{I_s \Delta t}{C_s + C_{gs}}\right]^2$$

$$N_o = \frac{g_m^2 \Delta t^2}{8C_o}\left[\frac{I_{ns} \Delta t}{C_s + C_{gs}}\right]^2 + \frac{I_{na}^2 \Delta t^2}{8C_o} \qquad (27).$$

This formula can be simplified further in the case that $C_g \gg C_s$. Further, the first term in equation 27 for N_o could be dropped with the assumption that noise from the amplifier by itself is significantly greater than the noise from the source of the signal.

In this case, after substituting all variables at equation 22 with those in equations 25-27 it could be seen that:

$$F_N = \frac{I_{ns}^2 g_m^2 \Delta t^2}{I_{na}^2 (C_s + C_g)^2} \qquad (28).$$

We can see that F_N is dependent on g_m^2/C_g^2 (again considering that $C_g \gg C_s$). Thus, to enhance F_N, g_m^2/C_g^2 must be large. This can be accomplished through the geometry of the JFET, as discussed above and in equation 29. The remaining terms in F_N (noise current -- I_{na}) are more complex in nature, and will not be considered beyond the brief discussion below.

As shown in articles "JFET-CMOS process . . ." by G. Cesura et.al[8]., "Design Considerations for Improving . . .", by J.W. Haslett, et. al[9]., and "Short channel, CMOS-compatible JFET in low noise applications", by W. Butler[10], in order to get lower noise in any semiconductor device, we must use a higher doping concentration for selected parts of the device. Since we should not use the abstract model of JFETs to try to design only small capacitance without considering the noise performance, we must consider high doping for the channel region, which will lower the 1/f noise. But there is a limit to how high the doping should be. It has been shown[11] that diffusion of high-concentration phosphorus will induce dislocations. In high concentration these imperfections form a network of edge-dislocations. It has been shown in theory that formation of these diffusion dislocations is related to the doping concentration gradient and doping concentration itself. The nature of such dislocations is connected to lattice mismatch, induced by the diffusant.

In "Moderate-temperature anneal of 7nm thermal . . ."[12], the authors show the importance of the annealing treatment for interfacial traps distribution. The results of their research show that a short annealing time at low temperature could cause a consistent increase of the interface trap density. It has also been shown that change in the technology of oxide growth will make a drastic difference in the interfacial traps concentration. The authors of this article also conclude that the distribution of defect centers will depend on the gases inside the chamber. They show that

annealing in argon at 700 C will increase defect density. They tied this observation to the presence of water vapor inside the chamber.

Acknowledging the breadth of the topic of optimal performance and noise, we will only consider the capacitance performance and explore the technique that will minimize damage to the crystal structure. These techniques include using a dry oxygen growth of silicon dioxide annealing crystal damage after implantation and aluminum sputtering; and using higher temperature for oxide growth and dopant diffusion. Many observations demonstrate that 1/f noise is tied to different impurities of metal in the silicon bulk, such as gold and copper, which often can be found inside the sputtering system chamber. This means that the system must be as clean as possible in order to help keep noise to a minimum.

5. Computer Generated Modeling

From the theory presented above, and after dividing equation 10 by equation 20, assuming that $x_{p2} - x_{p1} \approx a$, we can see that the ratio g_m/C_g is proportional to the following expression:

$$\frac{g_m}{C_g} \cong \frac{a^2 q \mu_n N_n}{l^2 \varepsilon_s} \qquad (29).$$

From this, we can see that in order to maximize ratio g_m/C_g, we must obey the following design rules: small junction depth for the gate (***a*** - the thickness of the channel should be high), high channel dopant concentration, and short l (the gate length). Note: the thickness of channel ***a*** is limited by the required pinch-off voltage at a value which will not cause a breakdown. We can also use material with higher mobility, such as gallium arsenide or germanium. But, since I had only a limited choice of available wafers, I limited my research to silicon wafers with 6μm phosphorus-doped epilayer with a dopant concentration of the channel at 10^{16}at/cm^3. I applied those guidelines in my computation modeling.

Due to limited resources, I chose a simple fabrication process. The steps of the process are as follows:

1. Create an isolation well by diffusing boron dopant into a wafer that has already had an initial phosphorus doping.

2. Create source and drain electrodes by diffusing phosphorus into the source and drain region of the wafer. This can be done with a simple technique using spin-on glass dopant.

3. Create a gate electrode by doping the gate region with boron. This can be done either

with the spin-on glass technique or by implantation.

4. Evaporate the metal on the surface of the wafer, and pattern it to make the source, drain, and gate electrodes. Annealing is an important part of this process.

5. An etching process will be used in each step.

Those are the same basic steps that I used to complete my computer modeling.

For computational modeling, I used Silvaco tools (Athena) software. Athena is Silvaco's 3D process simulation system. It can be used with any combination of OPTOLITH, ELITE, and SUPREM4. Atlas is also a Silvaco 3D device simulation system. A program called Deckbuild provides for use of both programs (Atlas and Athena) within a Windows environment. The results of these programs can be graphed on the Tony Plot program. All this software comes as a package, and all work together. Cheaper versions of the Silvaco Tools package, however, contain only Deckbuild, Athena, and Tony Plot. This latter package was the only one available for use at BYU and at MOXTEK facilities. I have been unable to test this model on electrical parameters since BYU didn't have a copy of the "Atlas" program, which is part of the "Athena" simulation program.

Time, pressure, temperature, doping concentration, silicon bulk doping concentration, and various environment types for the process were used as input parameters. The graphs of concentration and distribution in the bulk of material, and actual images of cross-sections of the device are the output parameters.

After performing the calculations with the "Athena" software, I could see that in order to create a shallow gate and still have high transconductance, we must use the following parameters for the fabrication technology. "Athena" shows that for the total conjunction (connection of the

upper boron doping with the boron from the substrate), for an isolation well formed in 5μm epilayer, we must use a **12-hour** temperature diffusion process at **1100 C**. In this case, the epilayer doping concentration was 10^{16} at/cm^3. The results of this simulation are shown in the following pages.

In Figures 6-9 are presented the results from calculations for boron isolation well diffusion. This diffusion is necessary in forming isolated, p-type wells. For this purpose, the boron impurity from the isolation doping should come in contact with the substrate boron, by means of diffusion. Figure 6 shows the situation when the boron dopant with initial concentration 10^{19} at/cm^3 is diffused for 600 minutes at 1100 C through the 6μm epilayer, n-type doped with $1.1 \cdot 10^{16}$ at/cm^3 concentration of phosphorus. From this simulation it can be seen that 600 minutes at 1100 C is not enough for contact to form between the boron-doped well and material doped by the boron diffusing up from substrate at 10^{18}at/cm^3. A gap of about 0.8μm of n-type material is still present.

Figure 7 shows the situation when the boron diffuses at 1100 C for 900 minutes. It can be seen that boron from the top diffusion begins to form a connection with the boron diffusing up from the substrate. Figure 8 presents the same type of isolation diffusion with a different concentration of boron in the substrate; 10^{17} instead of 10^{18} at/cm^3. It can also be seen that boron from the top provides a very solid connection with the substrate in 900 minutes of heating at 1100 C.

Figure 9 presents the same type of boron diffusion; when the diffusion time has been increased to 1020 minutes. The diffusion temperature is same -- 1100 C -- and the dopant concentration for the substrate of the wafer is $1 \cdot 10^{18}$at/cm^3. The concentration of phosphorus

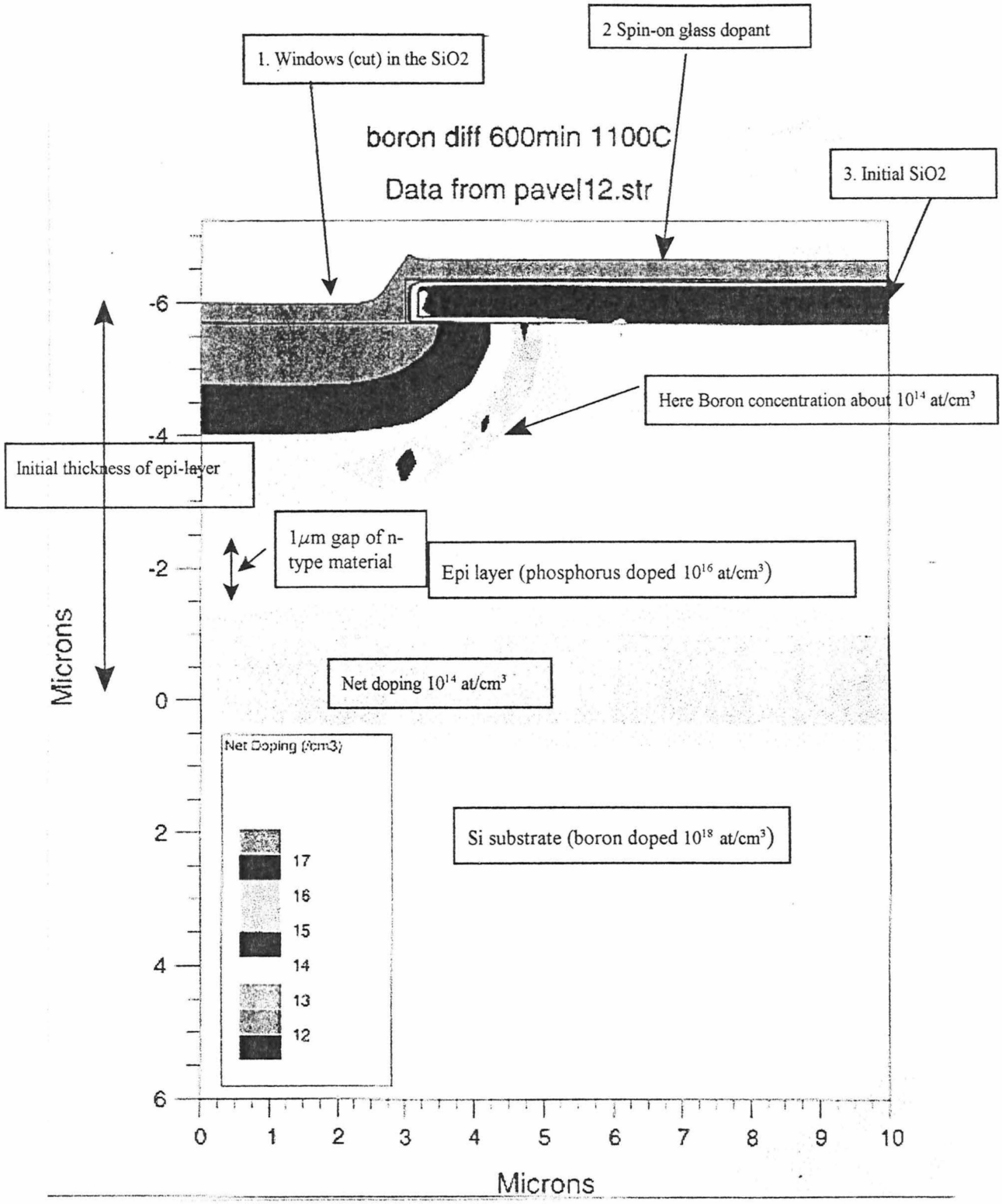


Figure 6. Boron isolation well formation. First attempt. Note that well formation is not complete; a gap of about .8μm of n-type material is still present.

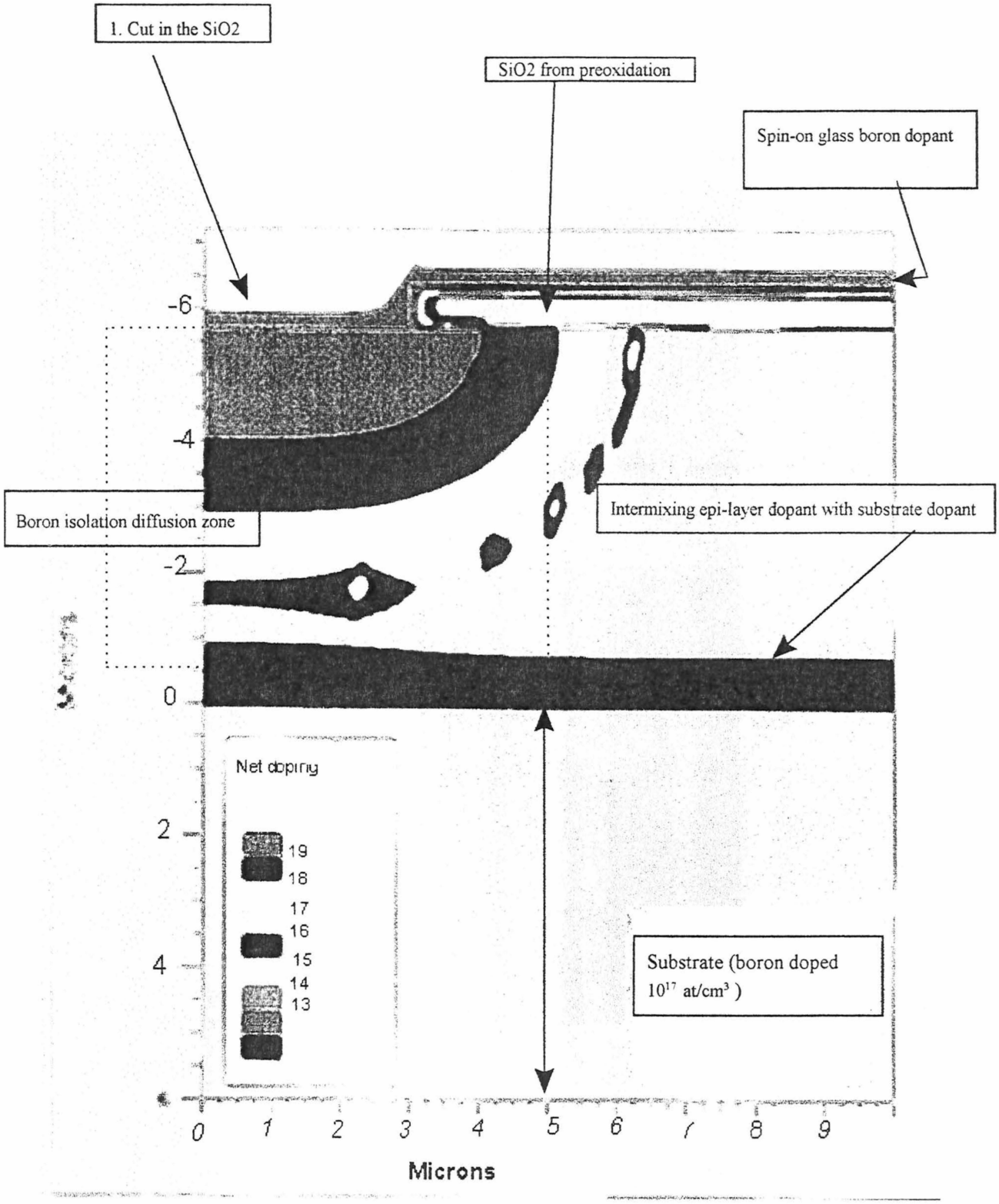


Figure 7. Boron isolation diffusion that has been done at 1100 C and for 900 min.

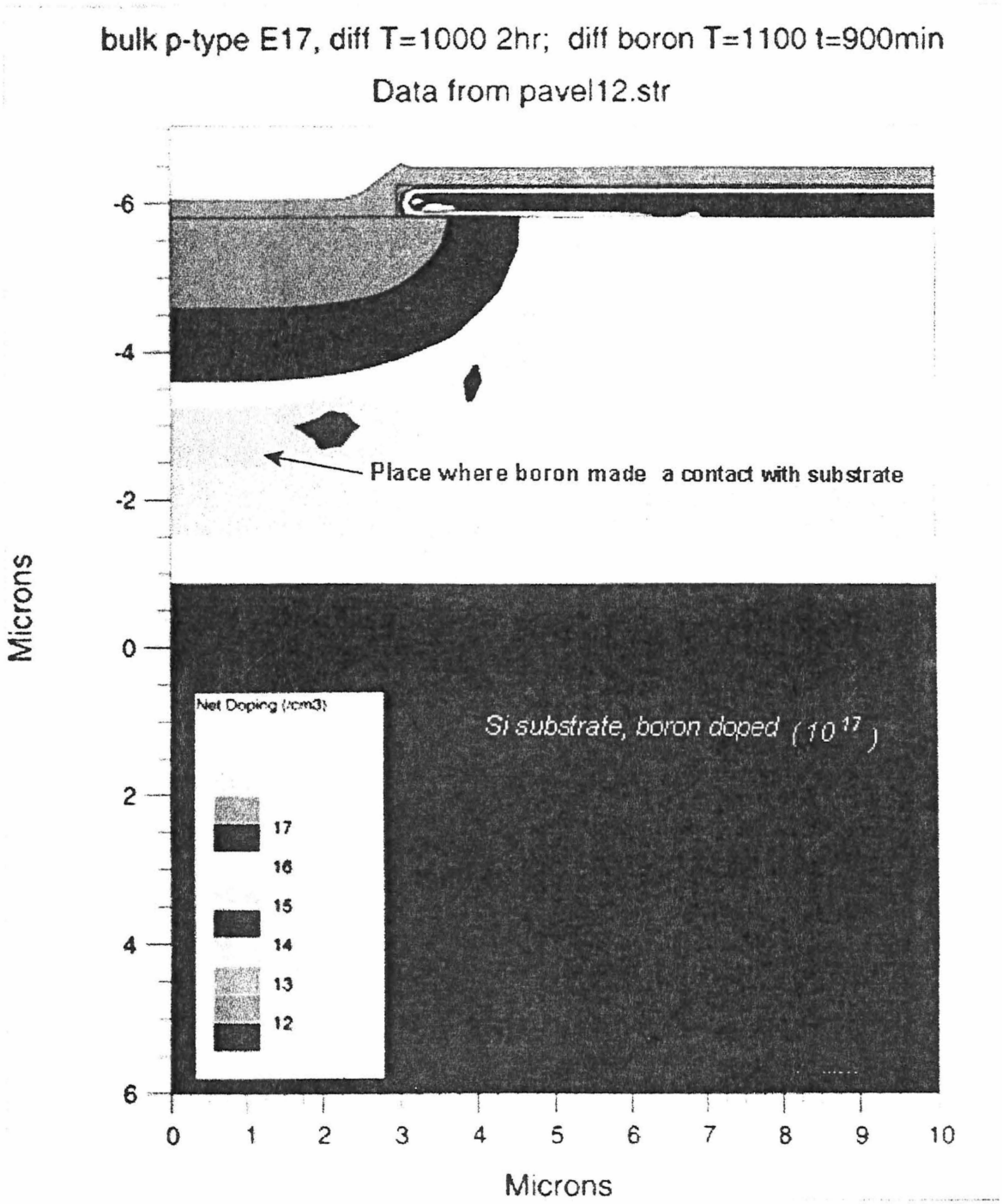


Figure 8. Boron diffusion for 900min at 1100 C with a substrate impurity concentration of 10^{17}at/cm^3. Contact has been achieved.

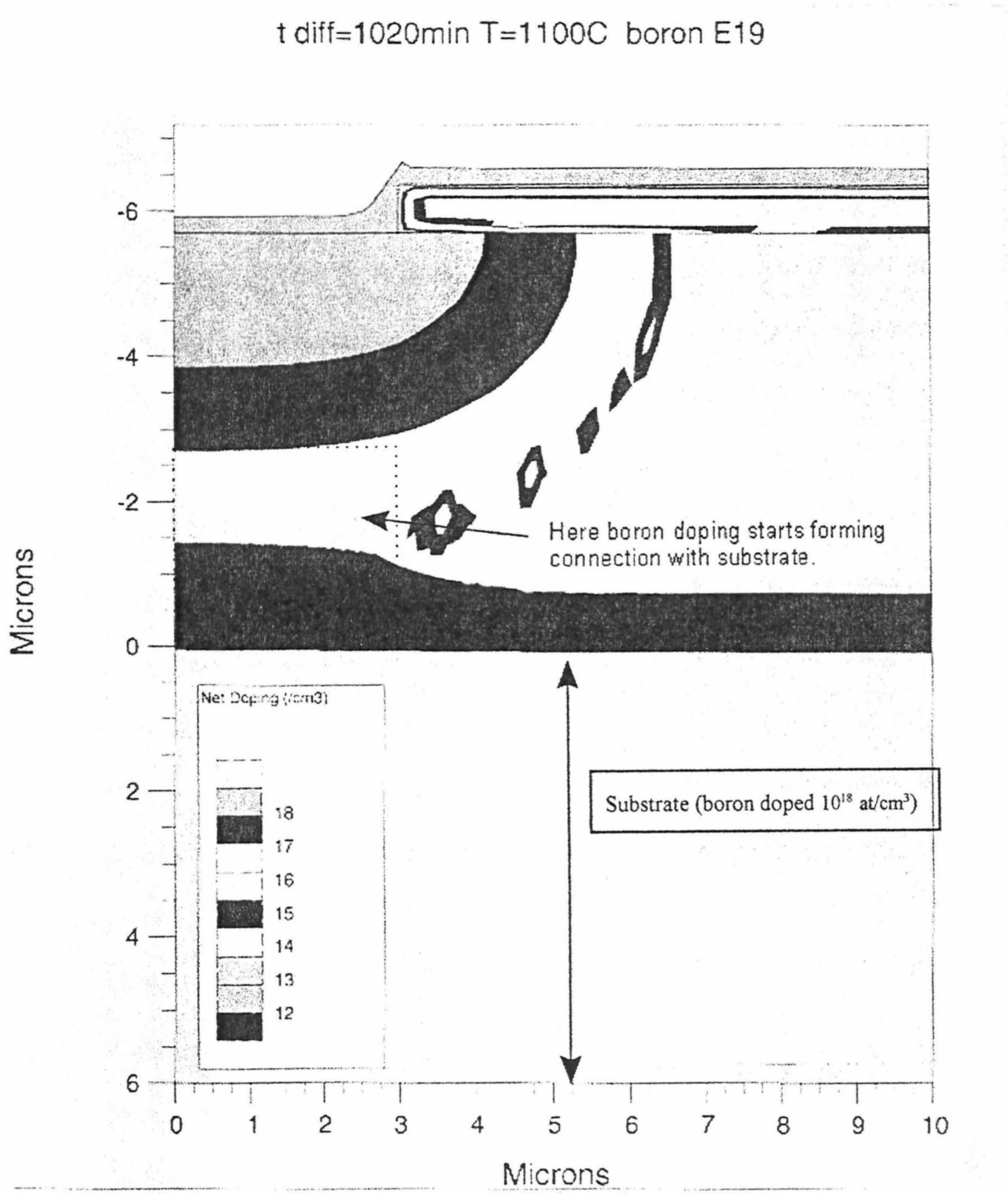


Figure 9. Boron isolation diffusion for 1020 minutes and 1100 C with a substrate impurity concentration of 10^{18}at/cm^3. Contact of top and bottom diffusions has been achieved. Isolation well has formed.

dopant in the epilayer is $1.1 \cdot 10^{16}$at/cm^3. From this figure we can see that the boron from the well doping came in contact boron from the substrate over a very wide region (at least 3μm in the x dimension). From this data we conclude that in order to form the electrical contact between the boron doped surface region and the substrate, through a 6μm epilayer of silicon doped with phosphorus at a concentration of $1.1 \cdot 10^{16}$ at/cm^3, we need to use a minimum of 12 hours of temperature diffusion at 1100 C. It should be mentioned that this 12 hour diffusion is the sum of the initial diffusion and all heating and diffusions of the source, drain, boron gate, and of oxidation for photo-lithography. Of these diffusions, the one which will have the greatest effect on forming this boron isolation well will be the source-drain diffusion at 2.5 hours. The oxidations of the wafers will also sum to approximately 2 hours for the total device processing. Thus, in order to begin fabricating an isolation well, we need to expose the wafer at 1100 C for t_{isol} = 12 hours - 2 hours - 2.5 hours $\approx$ 7.5 hours. 7.5 hours is the time required at the first part of the process to begin the isolation diffusion.

The next calculations were performed to investigate the proper conditions for the formation of the gate. There are four process parameters which can be varied:

1. The implantation energy
2. the dose
3. the annealing temperature
4. the annealing time.

In figures 10-12, we can see the calculations for boron ion implantation followed by diffusion into the silicon at conditions close to what I conclude is optimum. This simulation was performed with the following model: the substrate is doped with boron with initial concentration at

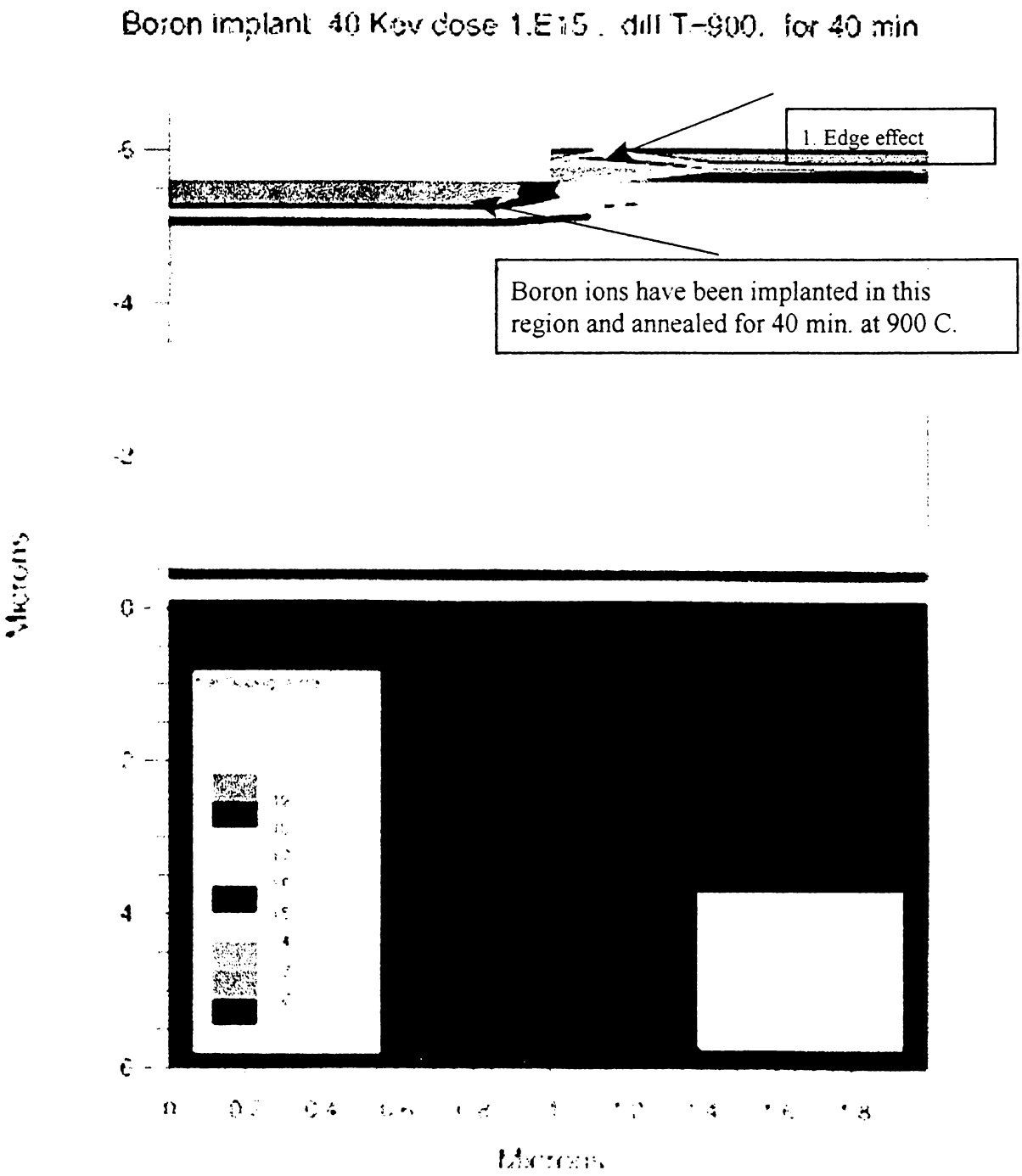


Figure 10. After boron implantation with 40 KeV and 10^{15} dosage boron ions and annealing

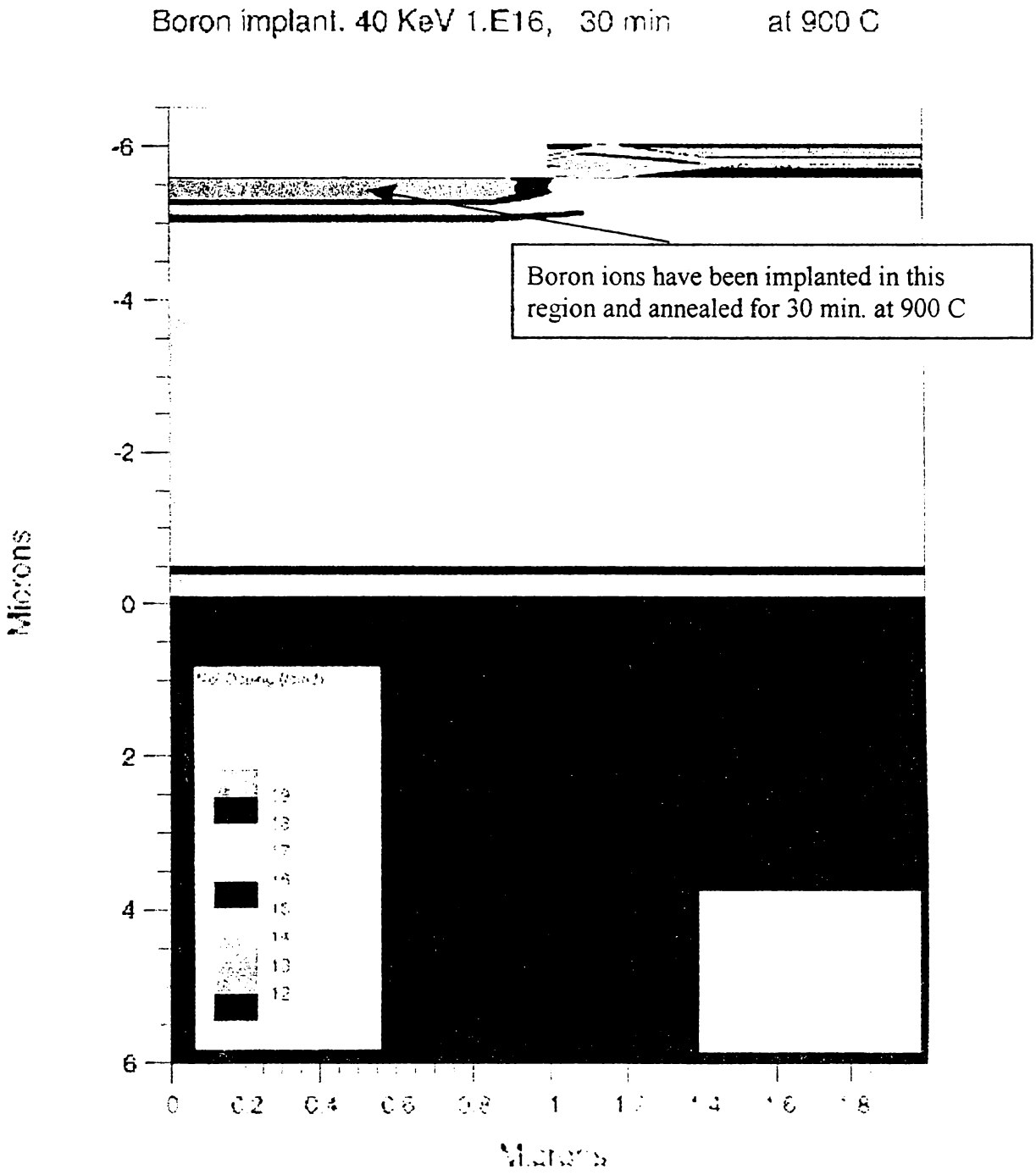


Figure 11. Structure of gate after boron ion implantation at 10^{16} at/cm^2 ion dosage and annealing.

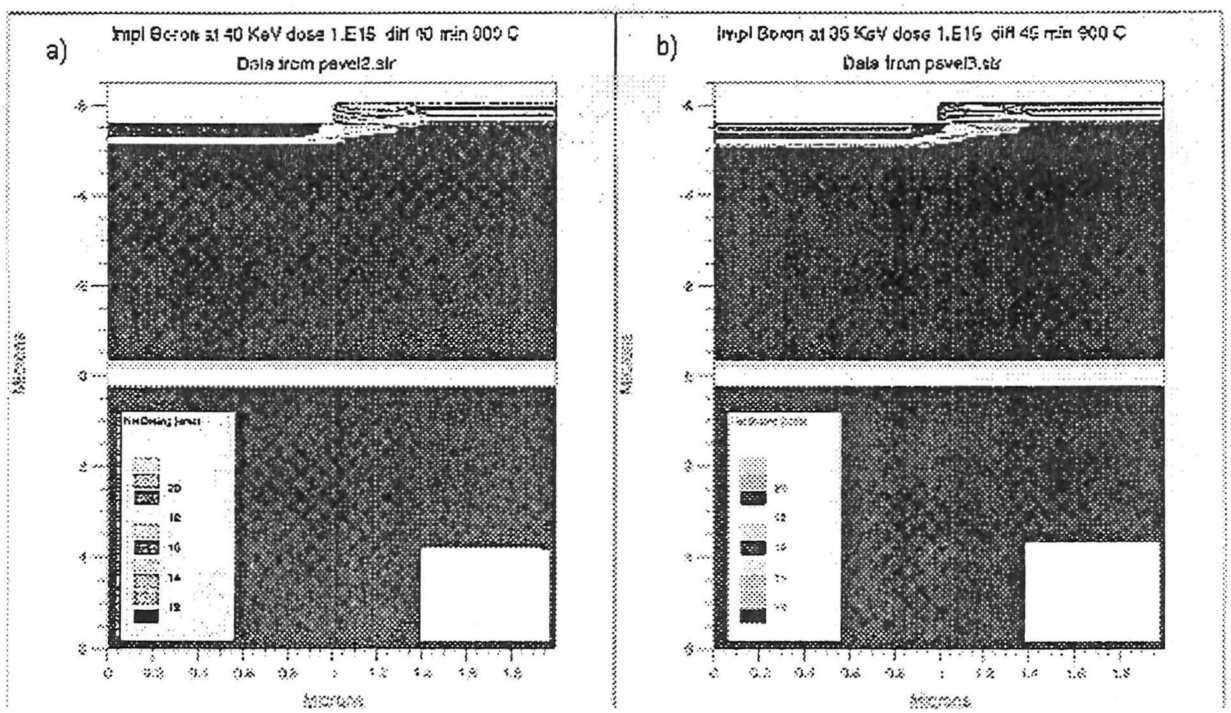


Figure 12. Side-by-side comparison of figures 10 and 11, showing a similar depth profile for boron dopant.

10^{18} at/cm^3, and a silicon epilayer doped with 10^{17}at/cm^3 phosphorus on top of the substrate. Figure 10 shows the completed cross-section of the wafer after boron ion implantation at 40 keV, with an ion dosage of 10^{15} at/cm^2. Annealing followed at 900 C for 40 minutes. In figure 11, we can see the same process as in figure 10, with a higher ion implantation dosage (10^{16} at/cm^2) and with an annealing performed for 30 instead of 40 minutes. We can see that there is very little difference between these two processes. Both graphs are displayed next to each other in figure 12 for better comparison.

Further variations in doping cross-sections due to dosage and primary ion energy, and

differences in the time and temperature of the annealing are shown in Figures 13-14. Figure 13a presents the initial wafer and distribution of the impurities. Figure 13b shows the cross section which develops at extreme conditions, when the ion dosage is higher (10^{17}at/cm^2), the implantation energy is higher (80 keV), the annealing time longer (120 minutes), and temperatures higher (1000 C). Figure 13c shows another extreme distribution of the impurities. The implantation energy is intermediate (56 keV), but the dosage is low ($8 \cdot 10^{14}$ at/cm^2), as is post implantation annealing temperature (550 C). The annealing time is 140 minutes.

Figure 14 contains three more simulations of ion implantation and annealing.. 14a shows a section of the device after 60 keV ion implantation with a 10^{15} at/cm^2 dosage and annealing at 1000 C for 60 minutes. Figure 14b shows the results after 80 keV, dosage $4 \cdot 10^{16}$, and annealing for 360 minutes at 800 C. The last graph on this figure, 14c, shows the results after implantation with high energy and dosage (90keV, 1x10^{17}ions/cm^2) with a subsequent anneal at intermediate conditions, 60 minutes at 900 C. From these simulations I conclude that in order to make a shallow gate with ion implantation, it is best to choose a low implantation energy (about 40 keV), as shown in Figure 11, with a dosage of 10^{16}at/cm^2, followed by a post-implantation anneal for 40 minutes at 900 C in an H_2 and N_2 atmosphere[13].

Figures 15-18 reflect the simulations for the complete device with the ion implantation for the gate electrode and phosphorus diffusion for source and drain electrode. The simulations also include subsequent sputtering and etching in aluminum on top of the device, (done in order to create the physical contacts with the electrodes). I show in figure 15, from left to right: 15a the initial wafer; 15b-c the source drain phosphorus diffusion, the only difference in the two being that b is a predeposition step and c is the beginning of the drive in diffusion; 15d the opening of the

contacts for the gate implantation; 15e the wafer before ion implantation, 15f the ion implantation with annealing; 15g the sputtering of aluminum on the surface and etching to form the contacts. 15h is a view of the device without showing the isolation boron diffusion.

Figure 16 shows the same type of process as in figure 15, with the emphasis on the boron isolation diffusion, and source-drain phosphorus diffusion. The simulation process used for phosphorus diffusion follow: spin on glass phosphorus dopant, open windows in the silicon oxide provide a path for the introduction of the dopant. The set time for predeposition is 30 minutes at 950 C. Then the spin-on glass dopant is etched off, and I perform a drive-in diffusion for 2 hours at 1100 C. Figure 16a-b (a being the source diffusion -- phosphorus dopant -- and b showing phosphorus diffusion with spin-on glass left on the surface) shows the profile after the phosphorus has been diffused into the wafer for 2 hours at 1100 C. 16c shows the oxide growing to prepare for gate formation, 16d shows the opening contacts for the gate implantation. 16e shows the cross-section after ion implantation and annealing; in 16f sputtered aluminum contacts have been deposited; in 16g the aluminum has been etched to form the patterned contacts. 16h shows the cross-section of the device at the end of this process of isolation diffusion near the edge of the isolation well. It is clear that the isolation well will have formed at this point.

Figures 17 and 18 show the devices after the above processes on a larger scale. In figure 17, the device has been completed by source-drain diffusion for 60 minutes at 900 C. Source and drain dopant diffusions are marked as 2 and 3, respectively, in figure 17. The gate – marked as 1, figure 17 – has been formed by ion implantation at 40 keV with a dose of 10^{17} at/cm^2 followed by annealing at 850 C for 4 hours.

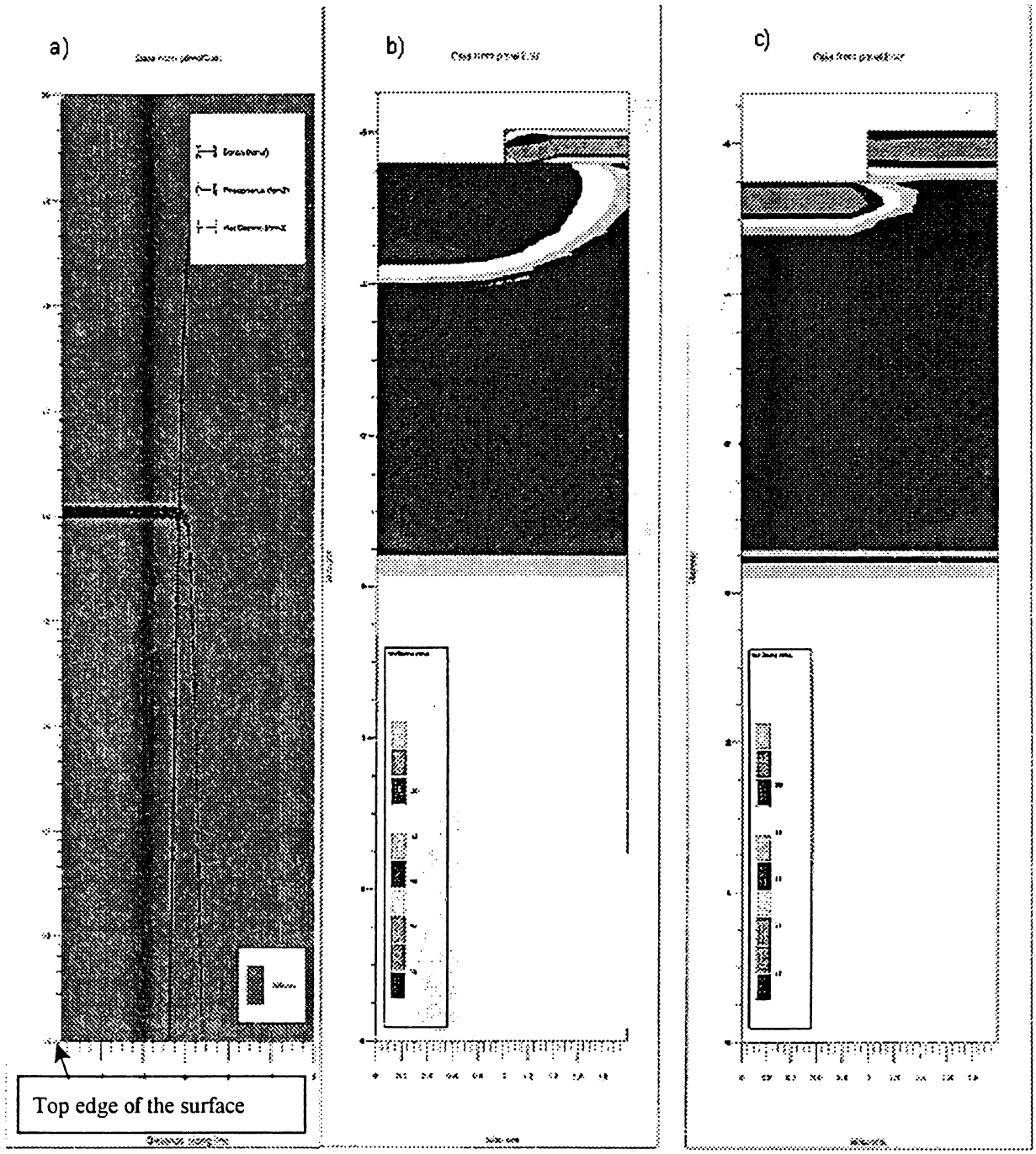


Figure 13. Boron implantation simulations for different primary ion energies. a) initial wafer. b) shows ion implantation dosage 10^{17}at/cm^2, energy at 80 keV, annealing time 120 minutes, and temperature 1000 C. c) shows implantation at 56 keV, dosage 8 x10^{14}at/cm^2, annealing time 360 minutes at 800 C. Note that the gray scale for these figures is the same as fig. 18 on p. 38.

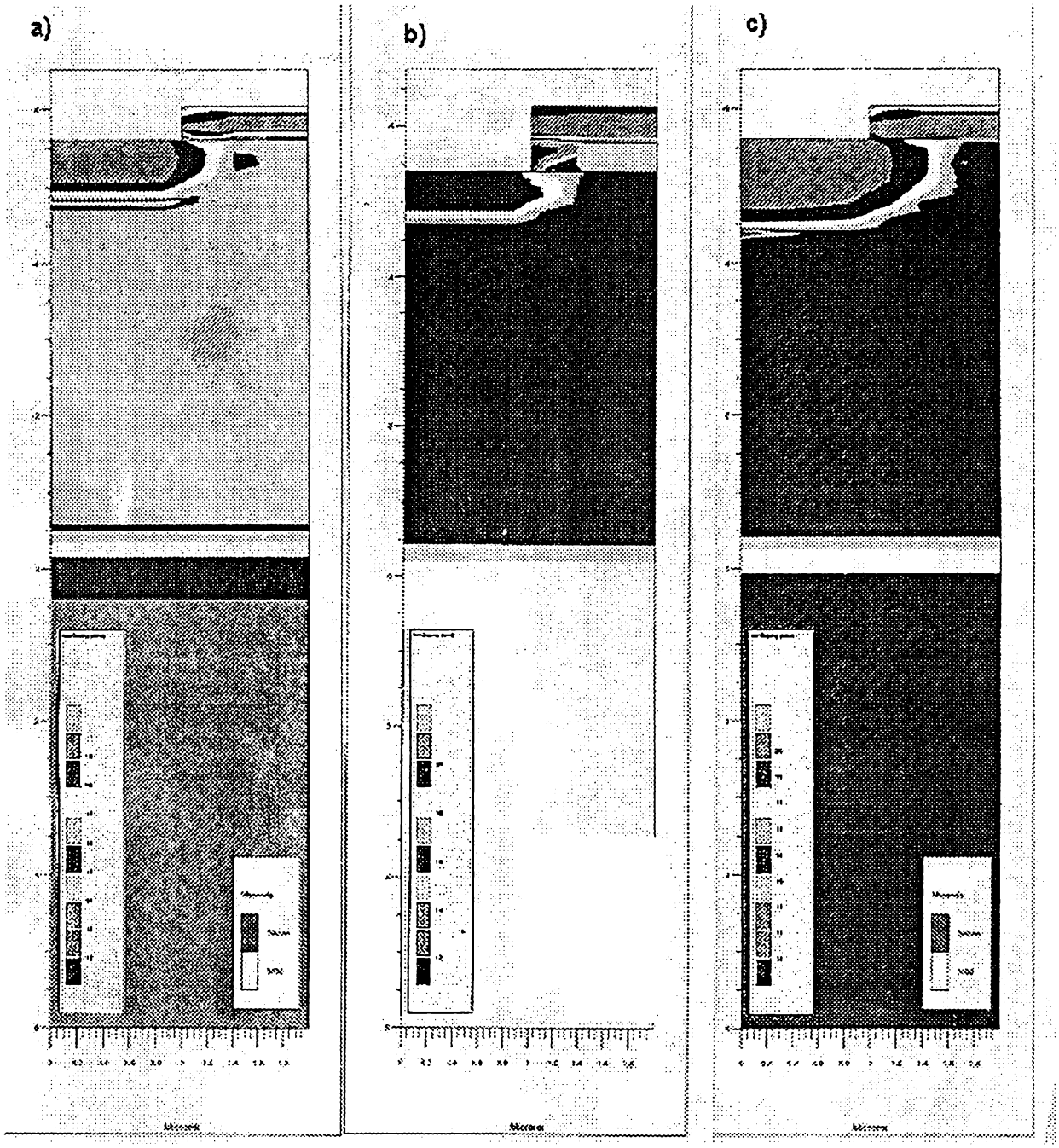


Figure 14. Further simulations of boron implantation for different primary ion energies. a) after 60 keV implantation with 10^{15}at/cm^2, annealing 1000 C for 60 minutes. b) after 80 keV implantation with 4 x 10^{16}at/cm^2, annealing for 360 minutes at 800 C. c) after 90 keV implantation with 1 x10^{17}at/cm^2, annealing for 60 minutes, 900 C. Note that the gray scale for these figures is the same as fig. 18 on p. 38.

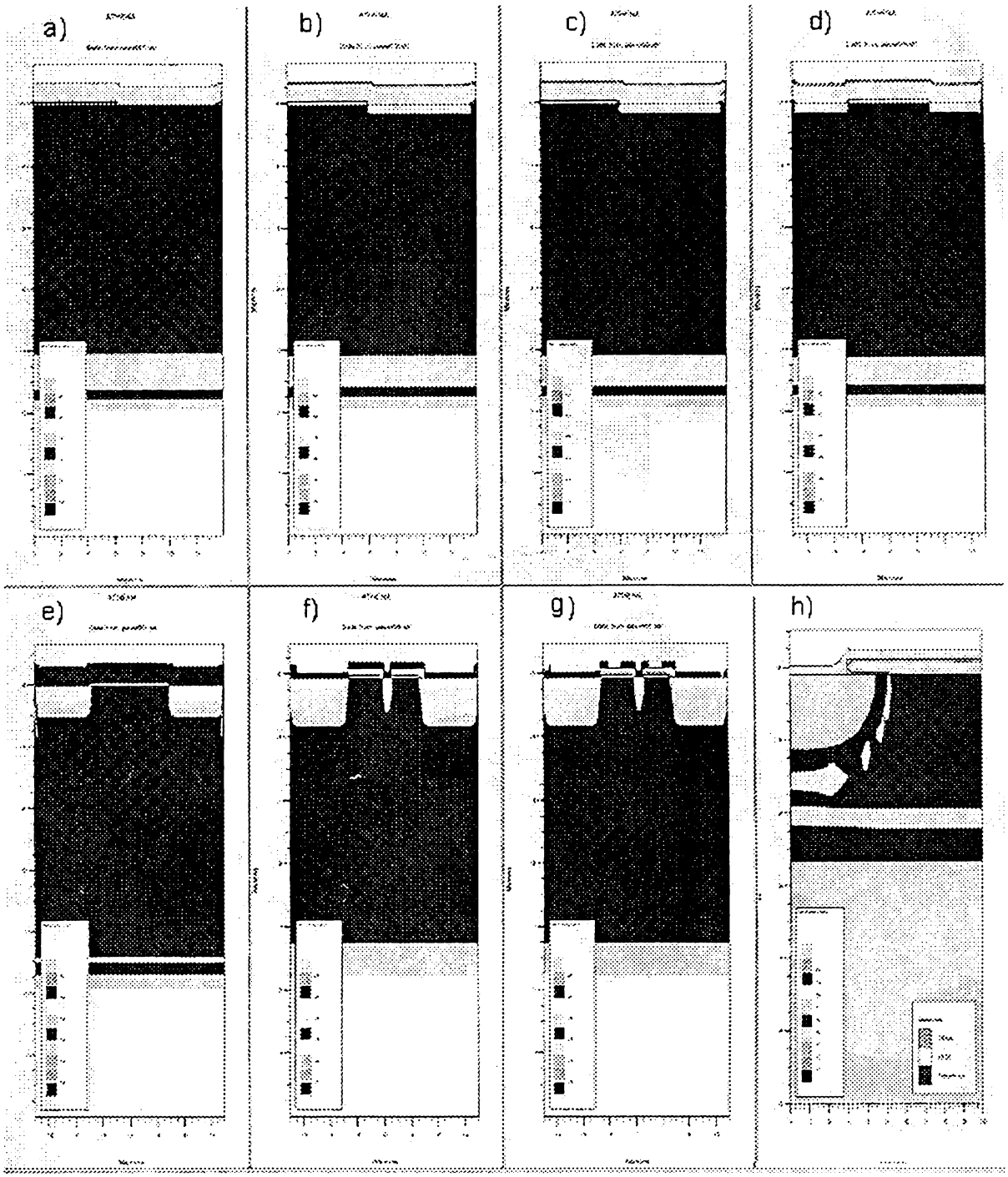


Figure 15. Device simulations when source drain (phosphorus) and gate (boron) diffusions have been performed (see text). Figure h) shows a cross section of the boron isolation diffusion at end of device formation. Note: The isolation connection has not been completely formed. Note that the gray scale for these figures is the same as fig. 18 on p. 38.

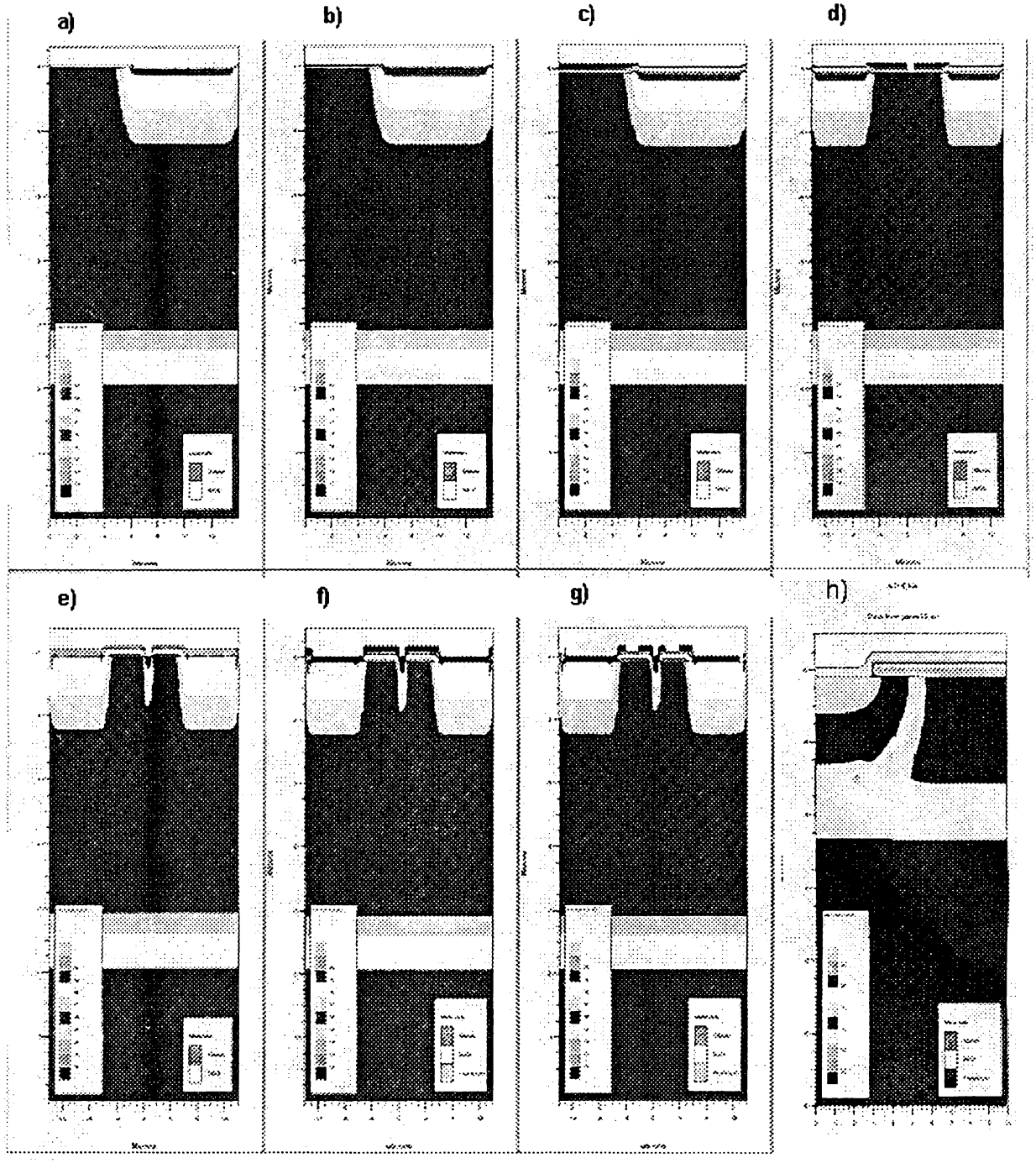


Figure 16. Similar simulations as in figure 15 (see text); the time for boron isolation diffusion well and for source drain diffusion have been increased. Note: There is no longer an isolation well gap. Note that the gray scale for these figures is the same as fig. 18 on p. 38.

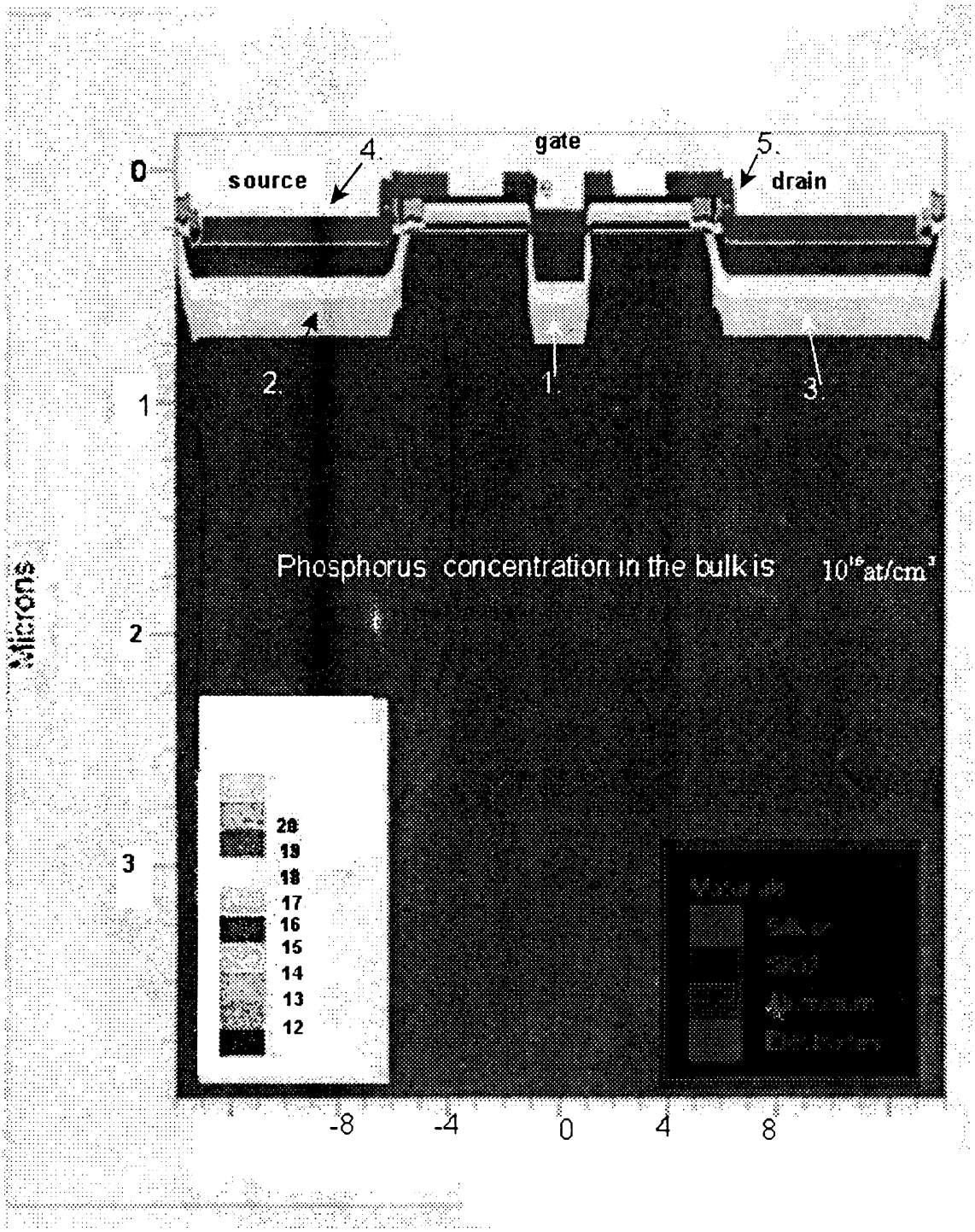


Figure 17. Final picture of the device after completing all process steps.

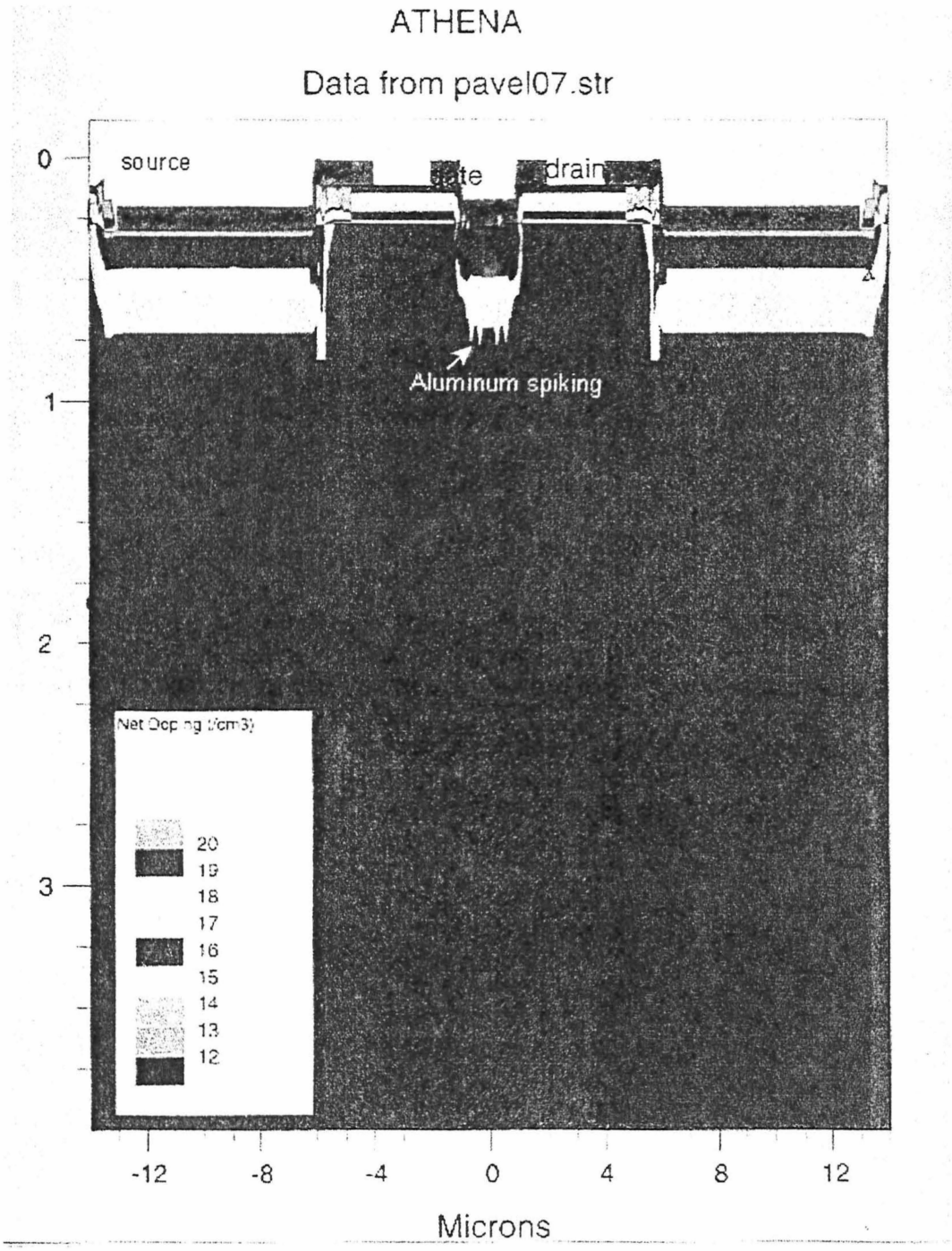


Figure 18. JFET's dopant distribution with aluminum spikes, formed by overheating during aluminum anneal.

Numbers 4 and 5 on figure 17 are source and drain aluminum contacts, respectively. In figure 18, we can see the device completed in the same manner as the previous one, but aluminum contacts have been annealed at 900 C for 20 minutes. We can see that the aluminum formed spikes; this will not be a functional device because those spikes create a short in the channel.

Aluminum spiking is a well-known problem, caused by a high coefficient of diffusion for aluminum in silicon[14]. To avoid this problem, it is necessary to sputter titanium as a buffer layer, or to anneal the aluminum at a low temperature before the eutectic point. Thus, for high risk devices (experimental samples), we need to use 550 C and 30 minutes for annealing aluminum. It is necessary to use annealing in order to activate aluminum atoms on the surface of the silicon. In the appendix of this thesis, starting on page 62, are presented the text actual programs that Athena used in its simulations. On page 62, we can see the program for ion implantation simulations. 63 shows the boron diffusion simulation program. Page 64 is the program text for simulation of the complete JFET.

6. Process description formulated on a base of "Athena" simulations

After the computer simulation and analysis of existing devices, I arrived at the process described below. Most of the following steps have been performed at the clean room in BYU's Department of Electrical Engineering. This clean room contains most of the equipment, however, it lacks an ion implanter and a sputtering system. Most of the chemicals were supplied by the Department of Electrical Engineering. The spin-on boron dopant was acquired fresh, since it quickly crystallizes in room temperature, and the previously available dopant had already solidified (use of this old dopant would have eventually caused formation of silicide, which is hard to etch).

I originally used masks that I made myself in the Department of Electrical Engineering. Due, however, to an inadequacy in size and clarity in creating a gate 2μm wide, I switched to masks obtained from MOXTEK.

The four-inch silicon wafers were also provided by MOXTEK. The substrate of these wafers contained a 10^{18}at/cm^3 boron dopant, and had a previously-grown epitaxial layer with $1.1 \cdot 10^{16}$at/cm^3 phosphorus dopant. The wafer was pre-cleaned in the clean room with HF. All of the following processes *must* be performed in the clean room, using the specified equipment, with safety and regulations necessary for semiconductor processing. Requirements for the deposition of the dopants (phosphorus or boron) placed special conditions on usage of the different apparatuses.

Part 1. Isolation well

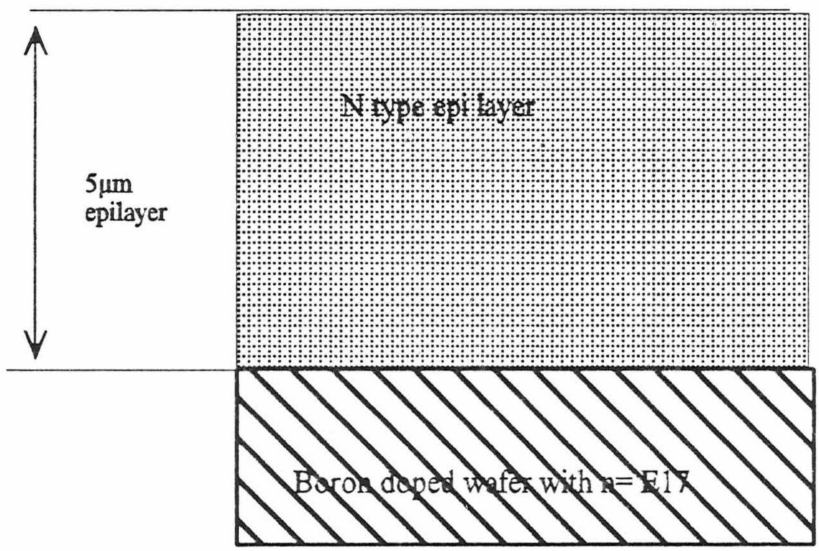


Figure 19: Initial wafer with 5μm epilayer, phosphorus doped ($1\cdot 10^{16}$ atom/cm^6).

1. Start with a clean, 4″ wafer with dopant concentration $N_{dwafer}= 1\cdot10^{17}$ at/cm^3 (boron doped) and epilayer with $1.6\cdot10^{16}$ at/cm^3, phosphorus doped. The thickness of the epilayer is 5μm. See Figure 19.

2. Oxidize at 1100 C for 120 min in additional 20% dry O_2 in the atmospheric ambient . The oxidation was performed in the clean room furnace. Tube number 2, which is set aside specifically for oxidizing wafers, was used in this case. Since theory indicated that dry oxide produces less noisy devices, we use flowing, dry oxygen gas in this step.

3. Spin the positive photoresist and apply the first mask. For this purpose, the BYU clean room has a special spinner. The spinning of the photoresist was performed at 4200 rpm. This process involves four steps:

a) Spin photoresist for 25 sec (standard positive photoresist).

b) Soft bake the wafer for 10 seconds at 95 C. This timing is very important for the developing; overbaking will cause nonuniform developing of the photoresist.

c) Expose photoresist on Perkin Elmer mask aligner with the first mask; no alignment is necessary. The Perkin Elmer (PE) machine projects the image of the mask onto the photoresist on the wafer, with the capability to align these masks to special marks on the wafer.

d) Develop the photoresist for ~65 seconds in the developer. All of these processes need to be performed in a yellow light environment. The quality of the developer has great influence on the quality of the image. Most of the failures I encountered during the fabrication of this device were connected to overused developer.

4. Harden the photoresist in the oven at 150 C for 30 minutes. It is necessary to make the photoresist hard enough to withstand an acid environment. This process is performed in an oven specially designed for this purpose.

5. Etch the oxide with BOE (buffered oxide etchant is a buffered HF in H_2O solution). The beakers with the solutions of HF are in the clean room. All necessary precautions with this hazardous material must be taken in this step.

6. Strip photoresist in the LFE stripper. This stripper is a plasma-etching machine that allows us to etch any organic material in an oxygen-plasma environment.

7. Spin on the boron dopant. This step is performed in the same spinner as in step 3, the spin rate and time as 2700 rpm and 40 seconds, respectively.

8. Predeposit the dopant by annealing at 950 C for 90 minutes in an N_2 atmosphere. This step was performed in the BYU clean room furnace set aside for this purpose. A special small furnace now functions in this capacity.

9. Deglaze (remove) the spin-on glass dopant in 10% BOE. This step is necessary in order to avoid formation of silicides on the surface of the wafer.

10. Measure the resistivity with a 4-point probe. This measurement will show us the dopant concentration of the measured area. According to the numbers, I could judge how well the previous steps had been executed.

11. Drive in diffusion at 1100 C for 10 hours in the small furnace tube with 35% N_2 and 65% air. The use of nitrogen gas in this step is included to prevent further oxidation of the wafer.

12. Remeasure the resistivity and analyze the depth of the boron dopant. In my fabrication, I

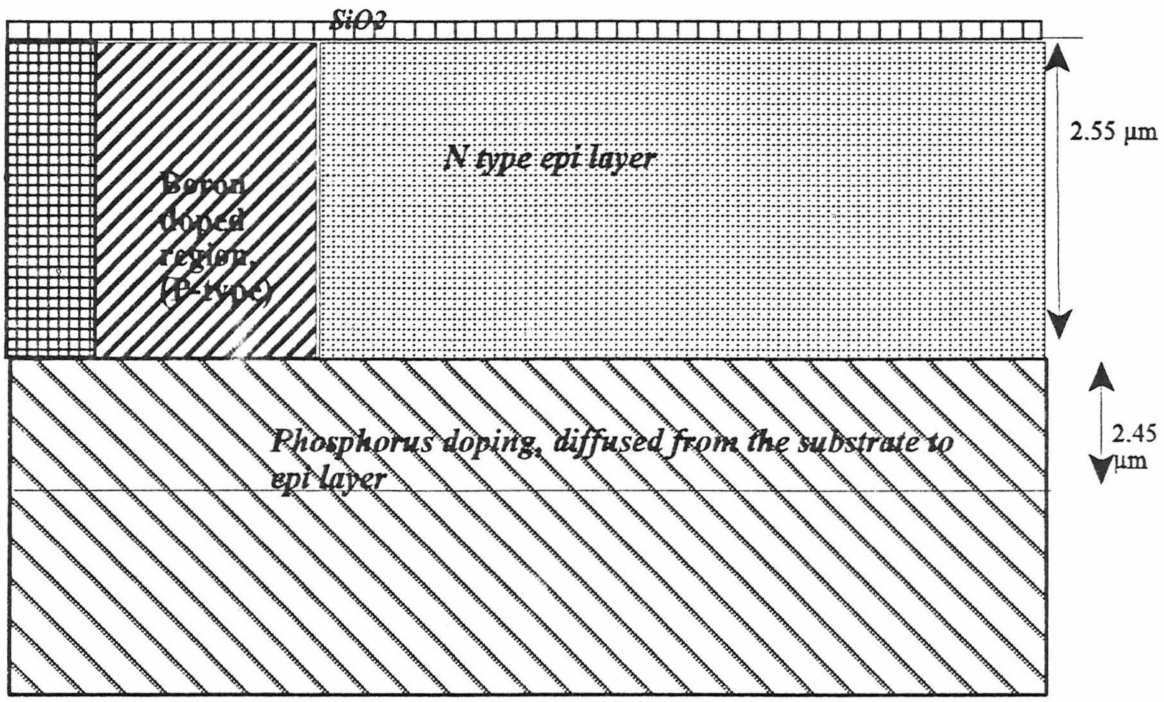


Figure 20: Boron isolation well formed by long timed diffusion.

noticed that after seven hours of drive-in diffusion, the sheet resistance dropped from 1.781 Ω/□ to 0.9Ω/□; after another four and a half hours of diffusion at the same temperature (1100 C) the sheet resistance became 11 Ω/□. That steep drop in the sheet resistance indicates that connection between isolation diffusion and substrate was achieved. Figure 20 shows a cross section of the designed device after this step.

Part 2. Source-Drain diffusion

Steps 1-4 of part 2 are the same as those in part 1. Thus, I will not spend time describing them in detail.

1. Re-oxidize the wafer for 20 minutes at 1100C. This step is the same as step 2, part 1 above, and is necessary because of the oxide etching performed in step 1 (part 1).

2. Spin on the photoresist and the pattern, using the second mask.

a) Spin on the photoresist for 25 seconds (standard positive photoresist).

b) Soft bake the wafer for 10 seconds 95 C.

c) Expose on Perkin Elmer with the second mask. Alignment is necessary in this step. The alignment marks were made during the first set of steps, as part of the first mask.

d) Develop the photoresist for ~65sec.

e) Hard bake photoresist in the oven 30 min.

3. Etch the oxide in the BOE.

4. Strip the photoresist , following the same procedure as in part 1.

5. Spin on the phosphorus dopant, using the clean room spinner at the same rpm (2700) as in part 1 for boron dopant.

6. Predeposit the dopant in the wafer by heating at 950 C for 90 minutes in N_2 atmosphere.

7. Deglaze the spin-on glass dopant in 10% BOE..

8. Measure resistivity with 4-point probe.

9. Drive in diffusion at 1100 C for 120 minutes in phosphorus tube with 35% N_2 , and 65% air.

10. Measure the resistivity and analyze the depth of the phosphorus dopant.

The cross section of the idealized device profile after this step is shown in figure 21.

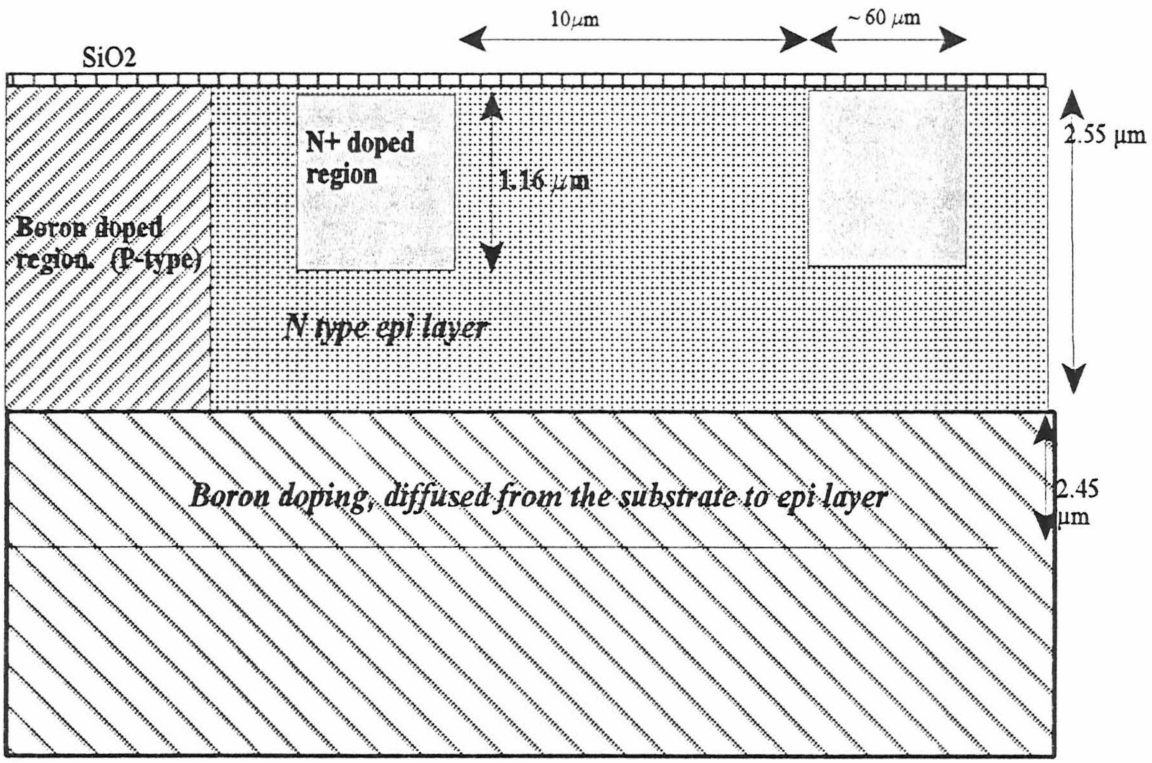


Figure 21: Phosphorus doped regions will formed SOURCE and DRAIN contact regions. This regions is responsible for forming the channel in the device.

Part 3. Gate Doping

1. Spin the photoresist and apply the third mask (the gate mask) using the Perkin Elmer aligner.

    a) Spin the photoresist for 25 seconds. This is a standard positive photoresist.

    b) Soft bake the wafer for 10 seconds at 95 C.

    c) Expose on the Perking Elmer aligner with the third mask.

    d) Develop the photoresist for ~65 seconds.

    e) Hard bake the photoresist in the oven for 30 minutes.

3. Etch the oxide.

4. Strip the photoresist.

5. Spin on the boron dopant.

6. Predeposition the dopant at 950 C for 20 minutes in N_2 atmosphere.

7. Deglaze the spin-on-glass dopant in 10% BOE..

8. Measure the resistivity and analyze the depth of the boron dopant.

The intended device cross-section after this step is shown in figure 22. For this step, a long, drive-in diffusion is not needed in order to form the gate, since the gate is supposed to be shallow, according to our design. After executing these steps and testing devices on functionality, I discovered that over-etching occurred in this process. Since there is little control over the etching technique in the BYU clean room, another method was used to form the gate electrode. Ion implantation could be used rather than the spin-on glass boron dopant. In this case, steps 5 and 6 were substituted by:

Alternative Part 3

5. Since BYU has no ion implanter, the wafers were sent to IION Corporation in California for

ion implantation. Implantation was performed with the following parameters: primary ion energy= 35 keV, tilt = 7 degrees, ion dose 10^{16} ions/cm^2.

6. Anneal damage to the crystal in the BYU clean room furnace. This step was performed for 30 minutes at 900 C.

Part 4. Opening Contacts

Since the following steps are the same as in parts 1 and 2, there will be few further detailed explanations.

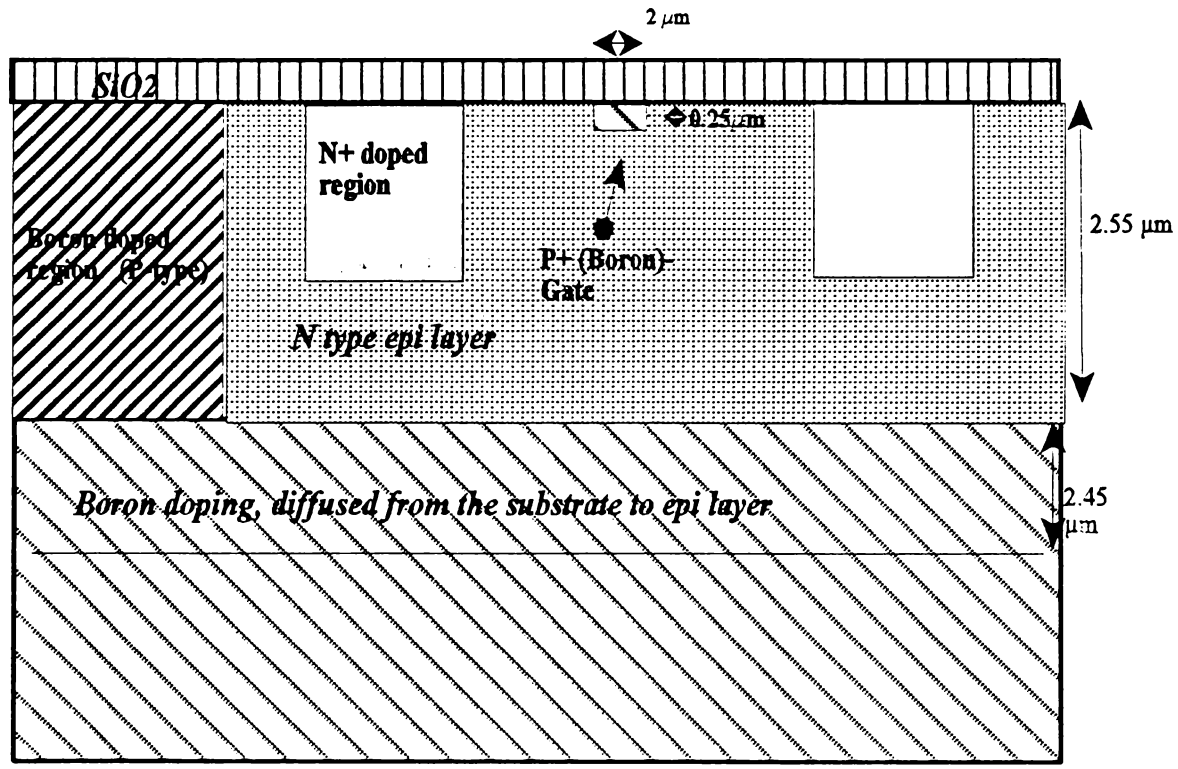


Figure 22: Boron doping for the forming of the GATE.

1. Spin on the photoresist and use the fourth mask to open contacts windows on the Perkin Elmer aligner.

a) Spin the photoresist for 25 seconds. This is a standard positive photoresist.

b) Soft bake for 10 seconds at 95 C.

c) Expose on the Perkin Elmer with the fourth mask, using alignment marks from the first mask pattern.

d) Develop the photoresist for ~65 seconds.

e) Hard bake the photoresist in the oven for 30 minutes.

3. Etch the oxide in the BOE.

4. Strip the photoresist.

Figure 23 shows how the device should appear at this point in its fabrication..

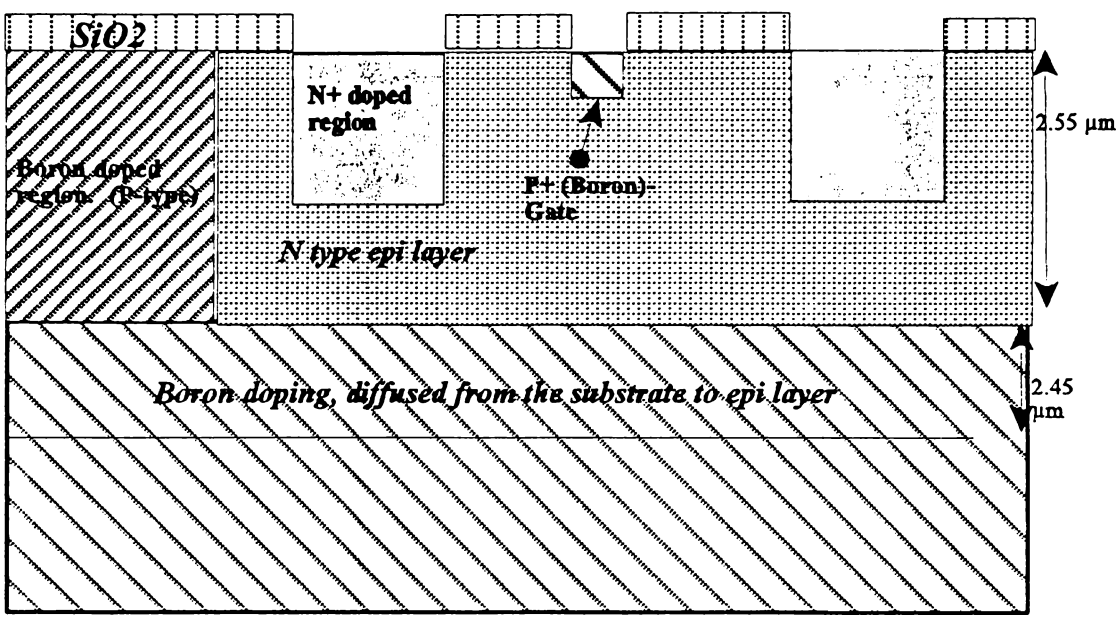


Figure 23. Opening for the metallization contacts.

Part 5. Evaporation Metals

1. Using the evaporator in the clean room, evaporate 0.1 μm Ti followed by 0.5 μm thick Al.

A picture of the device is shown in figure 24.

Alternative Part 5

Sputter with aluminum containing about 2% silicon to a 0.5 μm thickness.

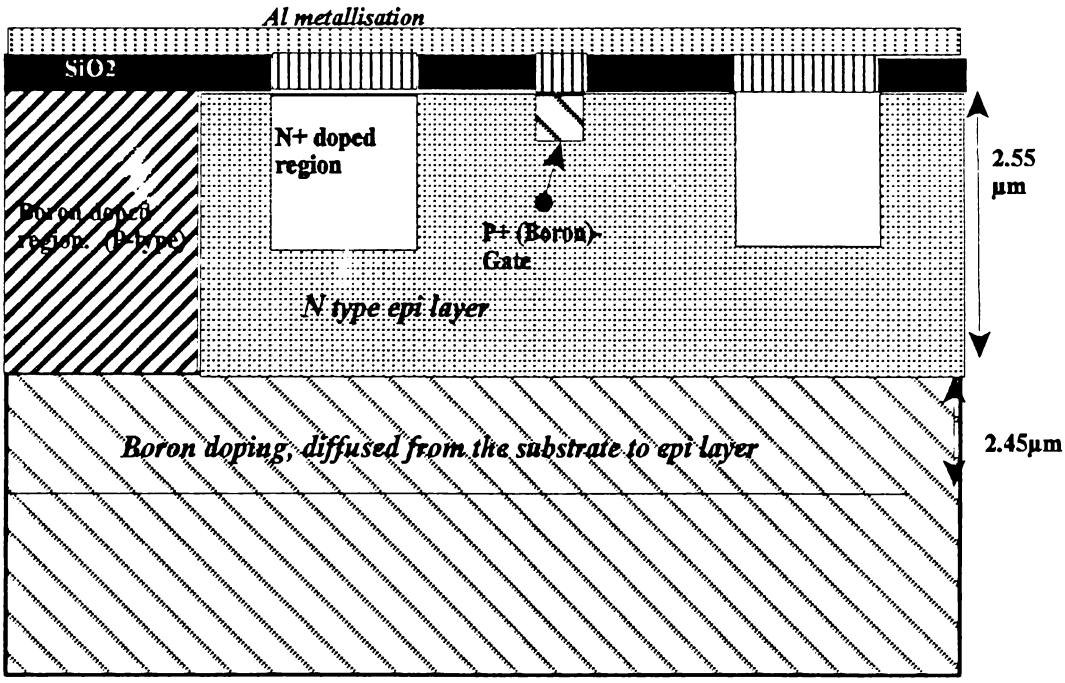


Figure 24 Aluminum metallization.

Part 6. Metal Contacts

1. Spin the photoresist and apply the fourth mask (contacts windows) on the Perkin Elmer aligner.

    a) Spin the photoresist for 25 seconds (standard positive photoresist).

    b) Soft bake 10 seconds at 95 C.

    c) Expose on the Perking Elmer with the fifth mask.

    d) Develop the photoresist for ~65 seconds.

    e) Hard bake the photoresist in the oven for 30 minutes.

2. Etch metal in 10% HCl.

3. Anneal in H_2/N_2 atmosphere for 20 minutes at 450 C.

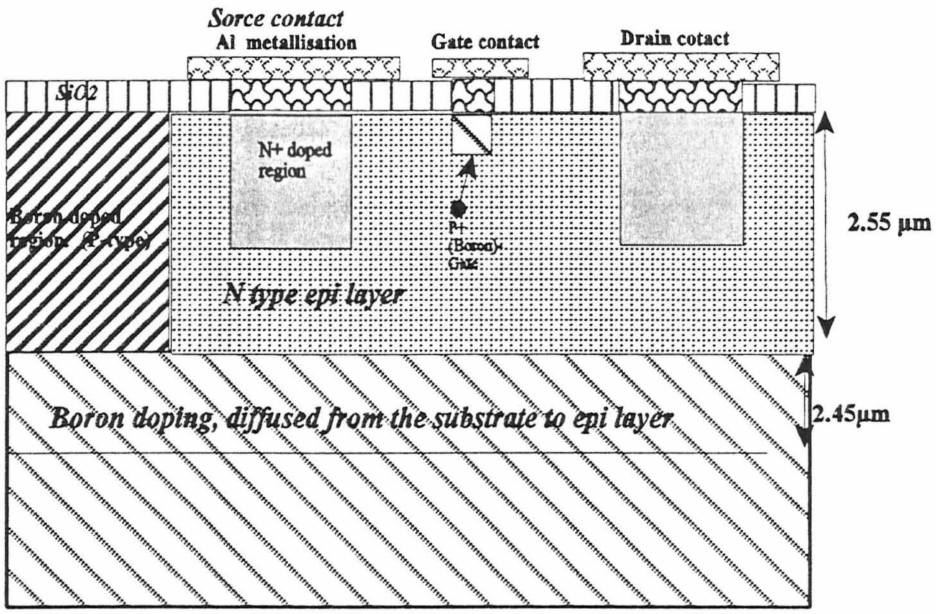


Figure 25 Cutting the Aluminum Contacts with the Last Mask.

Figure 25 shows a model of the actual device after completion of all steps.

7. Measurements of the junction profiles.

I made an analysis of a device that has been manufactured in Scotland with the masks provided by MOXTEK , and discovered the following parameters:

- The gate width is 2 μm.
- The distance between the gate and source or gate and drain is 4μm..
- The depth of the isolation well is 2.25 μm .
- The depth of the source (drain) diffusion is 1μm .
- The depth of the gate diffusion is 0.25 μm .

The last four measurements were obtained by 1° lapping and staining. Figure 26 shows such measurement after lapping and staining. I used the special fabricated jigs with a 0.1 μm diamond polishing paste, then the "reveal junction" stain. (This technique is very useful, as one does not need an SEM in order to see the junction profile.)

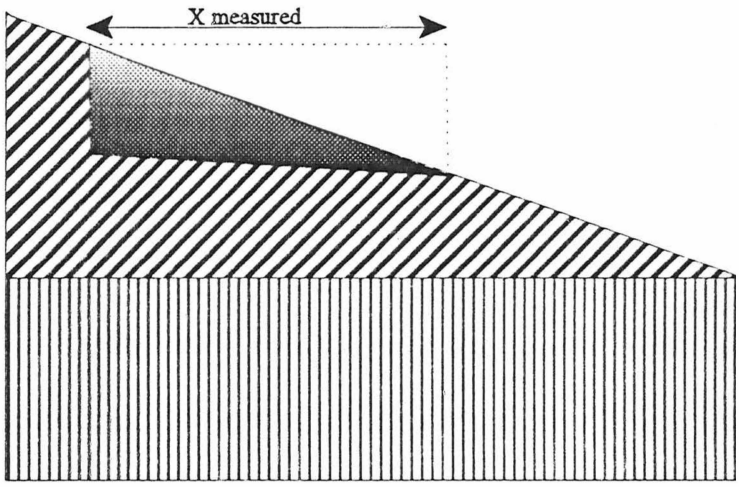
These procedures showed an isolation surface distance of X_{isol} =146.66 μm, which led by simple calculations to 146.66· tan (1)=255.9 E-2 μm =2.56 μm.
I used the required standard optical microscope for this measurement.

Description of Lapping and Staining Technique

The solution for the revealing and etching (DASH ETCH) of the doping profile consists of HNO_3 : HF : Acetic acid in respective proportions 3:1:12 . One must apply this solution for only 2- 10 seconds, otherwise the surface will be over-etched, and the 1° cut will have nonuniformity. The contrast will have optimum point in the specific time. Too much time in this etchant will

decrease the contrast. I determined that in my experiment the optimum ti
sec.

For lapping, the jigs are available for use in the BYU clean room.
polishing paste. Polishing was performed on the smooth side of the wafer



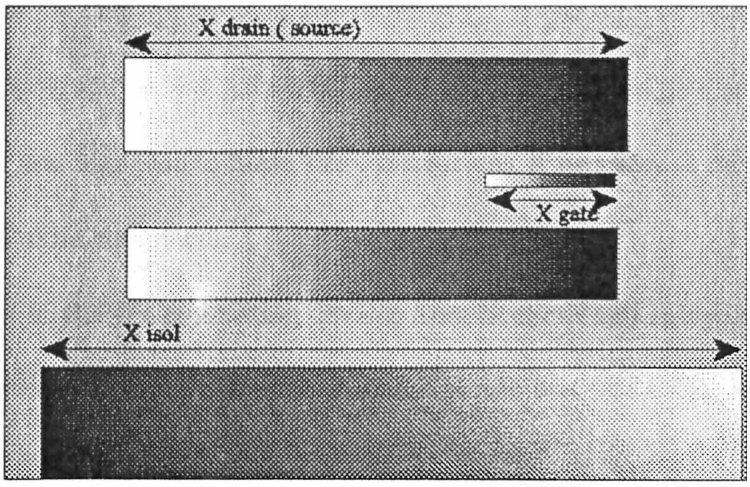


Figure 26: The measurement of the doping profile with lapping and staining technique.

8. Fabrication of the Device

Seven wafers were manufactured according to the process described above. Five of them, when completed, were nonfunctional. The first fabrication error was in using old developer, and in using buffered HF instead of concentrated HF. It is unusual, in theory, to need to use concentrated HF for etching spin-on glass dopant, but the real process shows that very short exposure in concentrated HF is much more effective than exposure in BOE. If BOE is used as an etchant for spin-on glass dopant, the device will be overetched.

Another mistake was using boron spin-on glass process for the gate doping, instead of using the ion implantation process. Since, again, we have little control over etching the spin-on glass, the devices had either an over etched gate – and because of that a shortened gate-to-channel distance – or underetched silico-boron, the result of which was a thin layer of spin-on glass between the aluminum contact and the gate dopant.

The third most common mistake was a misalignment of masks. Since the Perkin Elmer aligner would allow only alignment in the order of 1μ, it was difficult to achieve proper alignment. The smallest topography of the gate was 2μ, the space in between gate and source, and in between gate and drain, was 4μ. Due to these small dimensions, it was easy to mis-align the electrodes on the BYU clean room equipment.

In order to analyze preexisting devices from Scotland and compare them with my design, I treated them with lapping and staining technique. I also analyzed those devices by means of the measurement capacitance of the gate over the voltage, which gave me the profile of the doping. In the Appendix, pages 56 - 59 show the curve for gate capacitance over gate potential and the same machine analyzed those curves, recording the depth profile of the depletion layers. (Note that the

capacitance of the depletion layer will depend on the space charge distribution, and that the thickness of the depletion layer will depend on the gate voltage. This way, we can pull out the information regarding the dopant profile from gate capacitance over gate voltage). In appendix on pages 65-68, we can see that channel depletion of the device, MX11DG, has a gate depletion thickness, relative to the channel, of about 0.7μm.

During the process, a few additional measurements were performed. One of them was heat-probe testing. The physics behind the heat probe test are fairly simple. If we, by the means of a point source heater, heat up the tips of the voltmeter probe, we can see a change in the surface potential. This change is caused by the creation of electrons and holes (created by temperature) for different types of doping. The distribution of holes and electrons will vary depending on the majority carrier. We will note either a decreasing in the voltmeter reading from the surface potential difference, or an increase in that potential for n and p-type doping, respectively. Thus, if we have n-type material, and we heat the positive electrode, the positive potential rises. If, on the other hand, we heat the negative electrode, the reading on the voltmeter will go down. P-type material will exhibit in the opposite behavior. Namely, if we heat the positive electrode, the potential will decrease. By means of this simple measurement, I guaranteed that my doping deposition had been activated, and that it had a correct type.

The latest experiment was done on four wafers with the same initial parameters as described above. Two wafers had alignment problems due to the limitations of available equipment. The other two wafers were successfully processed until the gate formation step. During the proceeding steps small misalignments were observed. Those two wafers were subsequently sent to California for ion implantation with boron dopant at an energy of 35 KeV

and an ion dosage of 10^{16}at/cm^2. Before the wafers were sent to ion implantation, the oxide opening I observed to be close to the 2μm design.

After receiving the wafers from this process, steps 4-7 of the process description were completed. Electrical measurement showed the gates to be shorted. Microscopy revealed that the gates were not 2μm wide, but 3 or 4μm wide, and that there was a small misalignment of the gate electrode. The devices were nonfunctional. As was mentioned before, the misalignment is doe to equipment inadequacy. The increase in the gate width, however, is a characteristic of over etching. Perhaps this occurred at the implantation company.

9. Conclusion and Future Directions

There are three important aspects of creating a low capacitance, high gain junction field effect transistor for x-ray detectors. These aspects also suggest possibilities for further research.

In this thesis, I show that gate length l is one of the most important geometrical parameters for creating a low capacitance and high gain device. That parameter modeled by computer simulation gives us the fabrication parameters -- for example, the annealing times, temperatures, and dopant concentration -- necessary to successfully construct the device within specific JFET requirements. In order to manufacture a working JFET under these specifications, we need to have a gate length measuring less than 1μm. Therefore, the lithographer for mask projection must be capable of alignment within 0.5μm in order to reduce alignment error to less than 50%.

The second most important technological aspect concerns the etching technique. Even with alignment within 0.5μm, if the parameters of the etching process – such as temperature-to-chemical concentration of the etchant, etching time, and the thickness of the oxide – are not carefully controlled, the device cannot be successfully fabricated.

Third, the shallow gate suggested by the formula on page 20 of this thesis can only be achieved by using low energy ion implantation. The suggested energy is 35 keV, and suggested dosage is 10^{16} ions/cm^2.

My analysis of existing devices, manufactured in Scotland, led to an approximate value for the geometrical profile of the actual JFET. Those values gave me a base for my Athena simulations. Analysis of Athena simulations suggested specific parameters for doping time, doping concentration, and profile depths for the source drain and gate diffusions. Athena simulations

suggested ion implantation as one option among many to achieve a shallow gate. In reality, it was the only reliable method to achieve a shallow gate. The technological parameters derived by the simulations were only of limited assistance in construction of the JFET, possibly due to limited availability of equipment. As a result of trying those parameters in actual construction, I have been led to three areas of reasearch that it would be valuable to explore.

First, the aluminum spiking problem was touched on in my thesis, but the Athena simulations were inadequate. We need to find the best practical annealing temperatures, materials for the barrier layer, and annealing time. We also need to explore the use of materials other than aluminum – such as polysilicon.

Second, as this thesis has been concerned only with the gate capacitance question, it would be valuable to explore a simultaneous lowering of capacitance and noise. Theoretically, noise should drop when the gate is shortened. Changing the gate width should also improve capacitance parameters. At the same time, the practical issues surrounding creation of such a device might produce unexpected noise behavior. It could be valuable to try to optimize initial dopant concentration of the wafers, which will change the channel dopant. That parameter will alter the figure of noise, as well as changing the ratio g_m/C_g

Third, I find a need to explore the issues of changing basic semiconductor materials. Would it be better to replace silicon with either germanium or gallium arsenide? Theory and practical works claim that since the mobility in germanium is higher than in silicon, we could decrease the capacitance and increase the gain factor. Germanium was a basic semiconductor material during the early years of the industry, but has fallen out of use. It would be valuable to re-explore its properties and capabilities.

Endnotes

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```
go athena
#
line x loc=0.00 spac=0.30

line x loc=14.00 spac=0.30

#
line y loc=0.0 spac=0.1
line y loc=2.00 spac=0.50
#
#
init silicon boron resistivity=.01 orientation=100
#
epitaxy time=60 temp=900 thickness=5.0 press=1.00 c.phosphor=1.1e16

#
method fermi compress
diffus time=30 temp=1000 dryo2 press=2.00 hcl.pc=1.0
#
etch oxide start x=13.5 y=-5.03
etch cont x=13.5 y=-4.97
etch cont x=6.00 y=-4.97
etch done x=6.00 y=-5.03
#
#method adapt
#adapt.par silicon i.phosphor i.boron i.antimony i.silicon i.vacancy \
        max.err=4.00 min.err=1.0

#
method fermi compress grid.ox=.5
diffus time=40 temp=1120 f.n2=220.0 press=1.00 c.phosphor=1.0e19
#
#
#method two.dim viscous
#diffus time=30 temp=1000 f.h2o=100.0 press=1.00 c.phosphor=3.0e19

structure outfile=pavel01.str
#
method fermi compress
diffus time=240 temp=850 dryo2 press=1.00 hcl.pc=0
# save the structire
structure outfile=pavel02.str
method fermi compress
diffus time=10 temp=900 dryo2 press=1.00 hcl.pc=0
#
method fermi compress
diffus time=40 temp=900 weto2 press=1.00 hcl.pc=1
structure outfile=pavel03.str

#
struct mirror left
#
method fermi compress
diffus time=20 temp=900 dryo2 press=1.00 hcl.pc=0
#
etch oxide start x=-0.00 y=-5.072
etch cont x=-0.00 y=-4.83
etch cont x=1.00 y=-4.83
etch done x=1.00 y=-5.072

# save the structure
structure outfile=pavel04.str

#
implant boron dose=4.6e16 energy=15 crystal unit.damage dam.factor=1
#
```

```
method fermi compress
diffus time=360 temp=850 nitro press=1.00
structure outfile=pavel05.str
#
etch oxide start x=13.50 y=-5.26
etch cont x=13.50 y=-4.8
etch cont x=6.00 y=-4.8
etch done x=6.00 y=-5.26
#
etch oxide start x=-13.00 y=-5.26
etch cont x=-13.00 y=-4.8
etch cont x=-5.20 y=-4.8
etch done x=-5.20 y=-5.27

#
deposit alumin thick=0.10
#
method fermi compress
diffus time=20 temp=800 dryo2 press=1.00 hcl.pc=0
#
structure outfile=pavel06.str
#
etch aluminum start x=-4.00 y=-5.37
etch cont x=-4.00 y=-5.0
etch cont x=-2.20 y=-5.0
etch done x=-2.2 y=-5.37
#
etch aluminum start x=4.00 y=-5.37
etch cont x=4.00 y=-5.0
etch cont x=2. y=-5.0
etch done x=2. y=-5.37
#
etch aluminum left p1.x=-13.00
#
etch aluminum right p1.x=13.00
#

#
electrode name=gate x=0.00
#
electrode name=drain x=12.00
#
electrode name=sourse x=-10.00
#
structure outfile=pavel07.str
#
tonyplot pavel*.str
```

```
go athena
#

line x loc=10.00 spac=0.1

#
line y loc=0.2 spac=0.20
line y loc=6.00 spac=0.50
#
epitaxy time=30 temp=1000 thickness=0.50 press=1.00 c.phosphor=4.0e16
#
method fermi compress
diffus time=30 temp=1000 dryo2 press=2.00 hcl.pc=1.0
#
method fermi compress
diffus time=100 temp=900 weto2 press=1.00 hcl.pc=0 c.boron=1.0e17 \

#
deposit oxide thick=0.50
#
etch oxide start x=0.60 y=0.66
etch done x=8.54 y=0.66

structure outfile=pavel1.str
#
method fermi compress
diffus time=30 temp=1000 dryo2 press=1.00 hcl.pc=0
#
etch oxide left p1.x=1.00
#
implant boron dose=4.0e16 energy=80 crystal unit.damage dam.factor=1
#
method fermi compress
diffus time=120 temp=600 nitro press=1.00
# save the structure
structure outfile=pavel2.str
tonyplot pavel*.str
```

```
go athena
#
line x loc=0.00 spac=0.20

line x loc=11.00 spac=0.2

#
line y loc=0.0 spac=0.1
line y loc=2.00 spac=0.40
#
#
init silicon boron resistivity=.01 orientation=100
#
epitaxy time=60 temp=900 thickness=5.0 press=1.00 c.phosphor=1.1e16

#
method fermi compress
diffus ti   0 temp=1000 dryo2 press=2.00 hcl.pc=1.0
#
etch oxide sta   x=10 y=-5.13
etch cont x=10 y=-4.85
etch cont x=6.00 y=-4.85
etch done x=6.00 y=-5.13
#

#
#
deposit poly thick=0.50 c.boron=1.0e18

#


method fermi compress
diffus time=20 temp=800 dryo2 press=1.00
#
structure outfile=pavel01.str
#
etch poly all
#
tonyplot pavel01.str
```

```
go athena
#
line x loc=0.00 spac=0.30

line x loc=14.00 spac=0.30

#
line y loc=0.0 spac=0.1
line y loc=2.00 spac=0.50
#
#
init silicon boron resistivity=.01 orientation=100
#
epitaxy time=60 temp=900 thickness=5.0 press=1.00 c.phosphor=1.1e16

#
method fermi compress
diffus time=30 temp=1000 dryo2 press=2.00 hcl.pc=1.0
#
etch oxide start x=13.5 y=-5.03
etch cont x=13.5 y=-4.97
etch cont x=6.00 y=-4.97
etch done x=6.00 y=-5.03
#
#method adapt
#
deposit poly thick=0.30 c.phosphor=1.0e18

structure outfile=pavel01.str
#
method fermi compress
diffus time=240 temp=850 dryo2 press=1.00 hcl.pc=0
# save the structire
structure outfile=pavel02.str
method fermi compress
diffus time=10 temp=900 dryo2 press=1.00 hcl.pc=0
#
structure outfile=pavel03.str

#
struct mirror left
#
method fermi compress
diffus time=20 temp=900 dryo2 press=1.00 hcl.pc=0
#
etch oxide start x=-0.00 y=-5.072
etch cont x=-0.00 y=-4.83
etch cont x=1.00 y=-4.83
etch done x=1.00 y=-5.072

# save the structure
structure outfile=pavel04.str

#
implant boron dose=4.6e16 energy=15 crystal unit.damage dam.factor=1
#
method fermi compress
diffus time=360 temp=850 nitro press=1.00
structure outfile=pavel05.str
#
etch oxide start x=13.50 y=-5.26
etch cont x=13.50 y=-4.8
etch cont x=6.00 y=-4.8
etch done x=6.00 y=-5.26
#
etch oxide start x=-13.00 y=-5.26
```

```
etch cont x=-13.00 y=-4.8
etch cont x=-5.20 y=-4.8
etch done x=-5.20 y=-5.27
#
#
tonyplot pavel*.str
```

1.63E+17	0.101343
1.69E+17	0.109097
1.87E+17	0.115822
2.14E+17	0.121401
2.53E+17	0.126091
2.70E+17	0.129757
2.77E+17	0.133658
2.87E+17	0.136932
2.76E+17	0.140405
3.02E+17	0.143784
3.46E+17	0.146527
3.85E+17	0.149021
4.09E+17	0.151156
4.51E+17	0.15331
3.99E+17	0.154994
3.46E+17	0.15759
4.18E+17	0.161836
4.42E+17	0.16544
5.54E+17	0.169081
5.60E+17	0.171131
4.97E+17	0.174597
4.21E+17	0.177256
3.05E+17	0.181676
2.44E+16	0.184159
8.21E+16	0.234045
1.15E+18	0.313947
1.08E+17	0.317805
1.20E+17	0.321669
1.72E+17	0.326869
1.74E+17	0.331128
1.84E+17	0.336065
2.09E+17	0.3397
2.01E+17	0.343538
2.20E+17	0.347369
2.90E+17	0.351767
2.98E+17	0.356113
2.77E+17	0.361761
2.96E+17	0.366707
3.32E+17	0.37154
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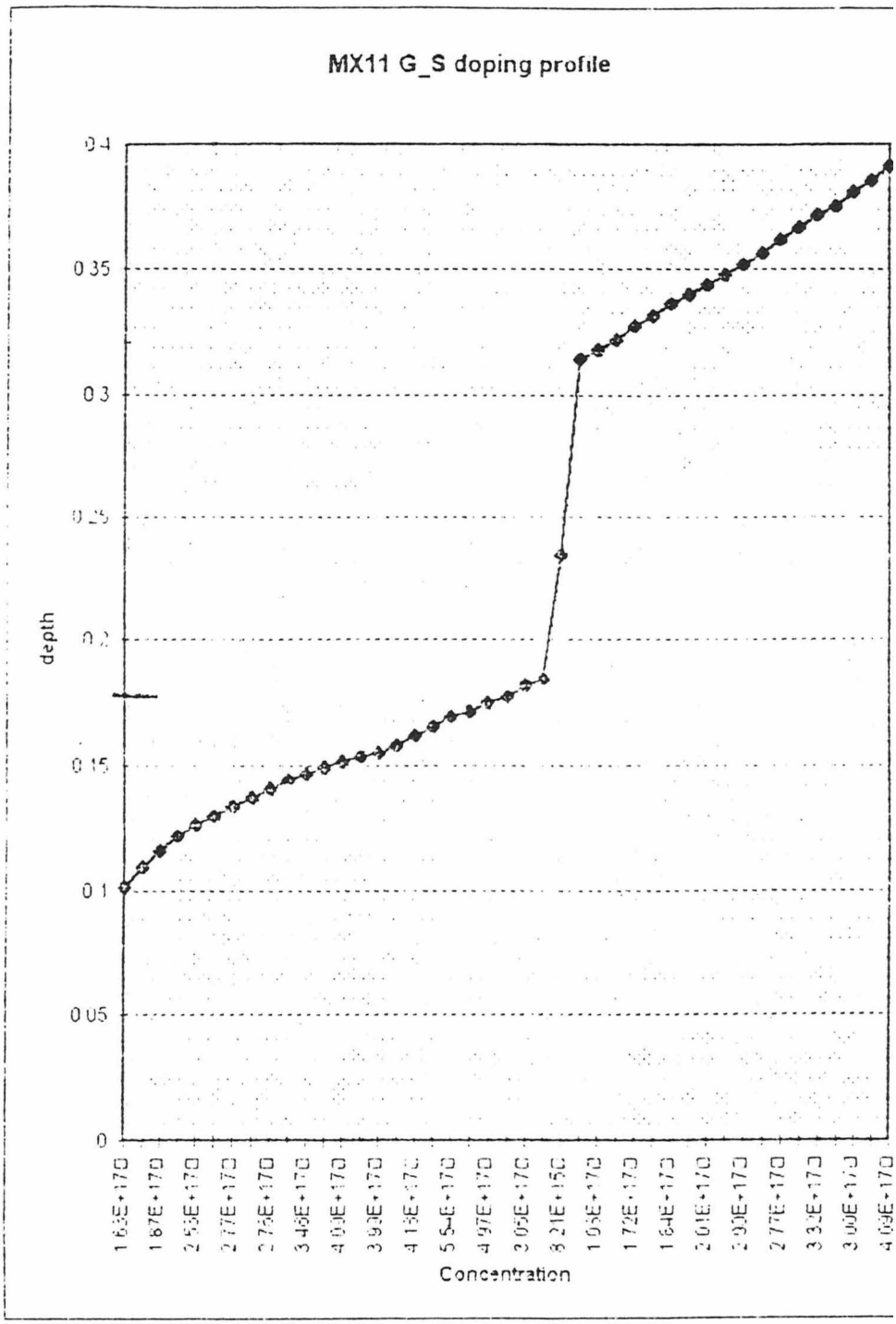
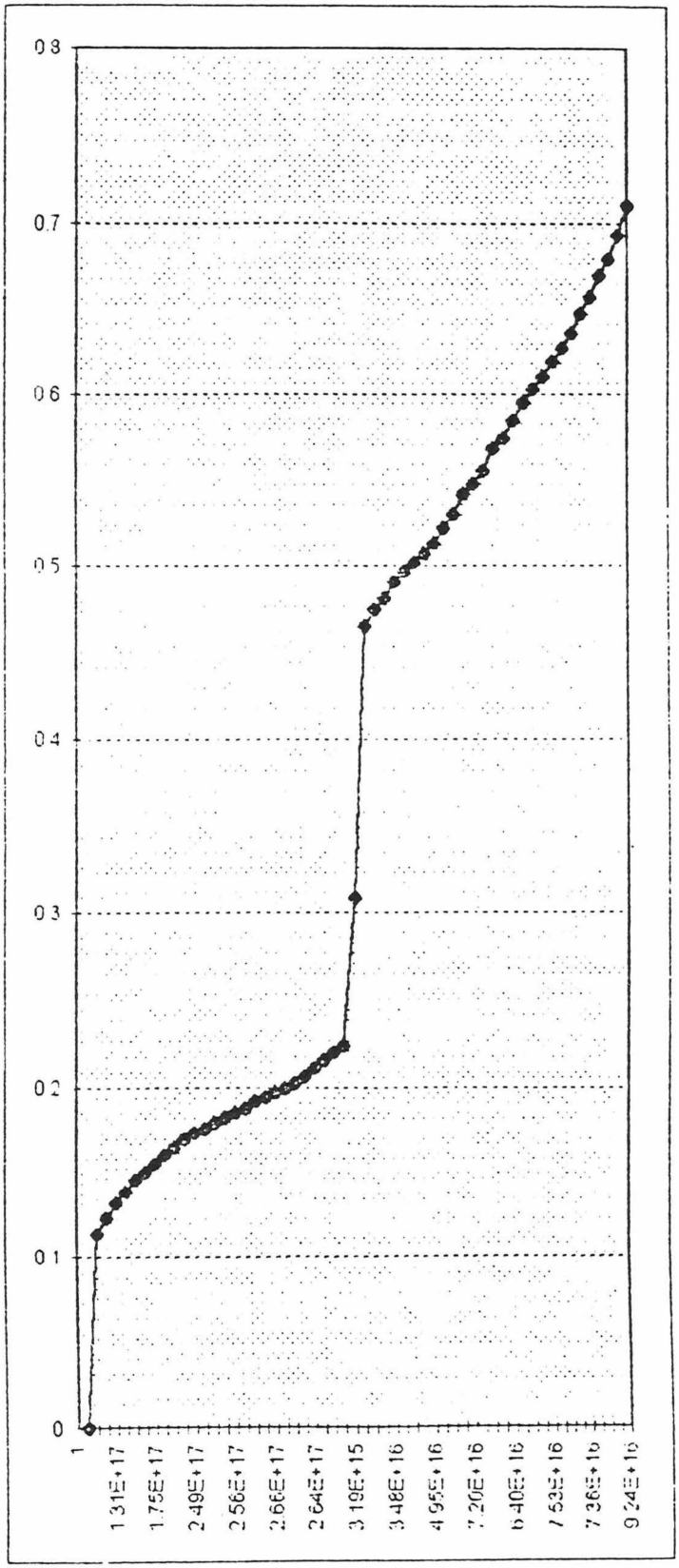
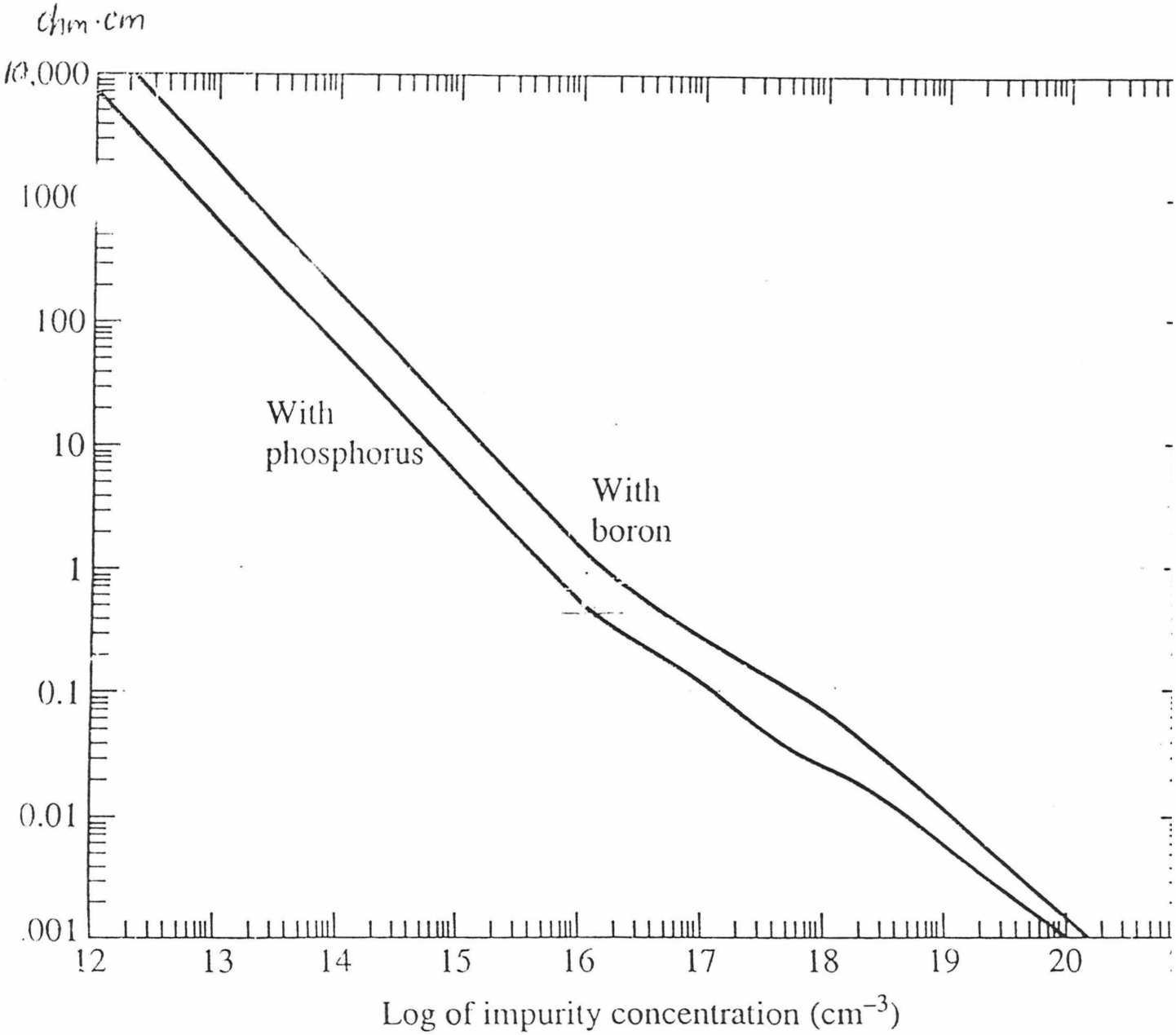


1

DOPING	DEPTH
1.23E+17	0.113668
1.21E+17	0.122776
1.31E+17	0.131528
1.44E+17	0.138243
1.60E+17	0.144876
1.74E+17	0.149756
1.75E+17	0.155062
1.77E+17	0.159554
1.64E+17	0.164433
1.86E+17	0.169365
2.49E+17	0.172892
2.61E+17	0.175553
2.40E+17	0.178664
2.43E+17	0.18174
2.56E+17	0.184683
2.08E+17	0.187049
2.15E+17	0.191479
2.54E+17	0.193812
2.66E+17	0.196853
2.83E+17	0.198898
2.74E+17	0.201561
2.85E+17	0.205036
2.64E+17	0.210582
2.70E+17	0.214911
2.81E+17	0.21972
8.81E+15	0.223521
3.19E+15	0.307768
4.07E+15	0.465128
3.58E+16	0.474557
3.44E+16	0.48078
3.48E+16	0.490529
4.78E+16	0.496392
4.91E+16	0.501723
4.68E+16	0.507147
4.95E+16	0.512893
6.17E+16	0.521293
5.00E+16	0.52939
5.47E+16	0.541261
7.20E+16	0.547397
6.09E+16	0.554709
7.50E+16	0.567644
8.19E+16	0.573516
6.40E+16	0.58451
7.30E+16	0.594802
8.61E+16	0.602879
8.21E+16	0.610149
7.53E+16	0.618751





electrical resistivity of silicon vs. impurity concentrations at 300 K. (After [R1-